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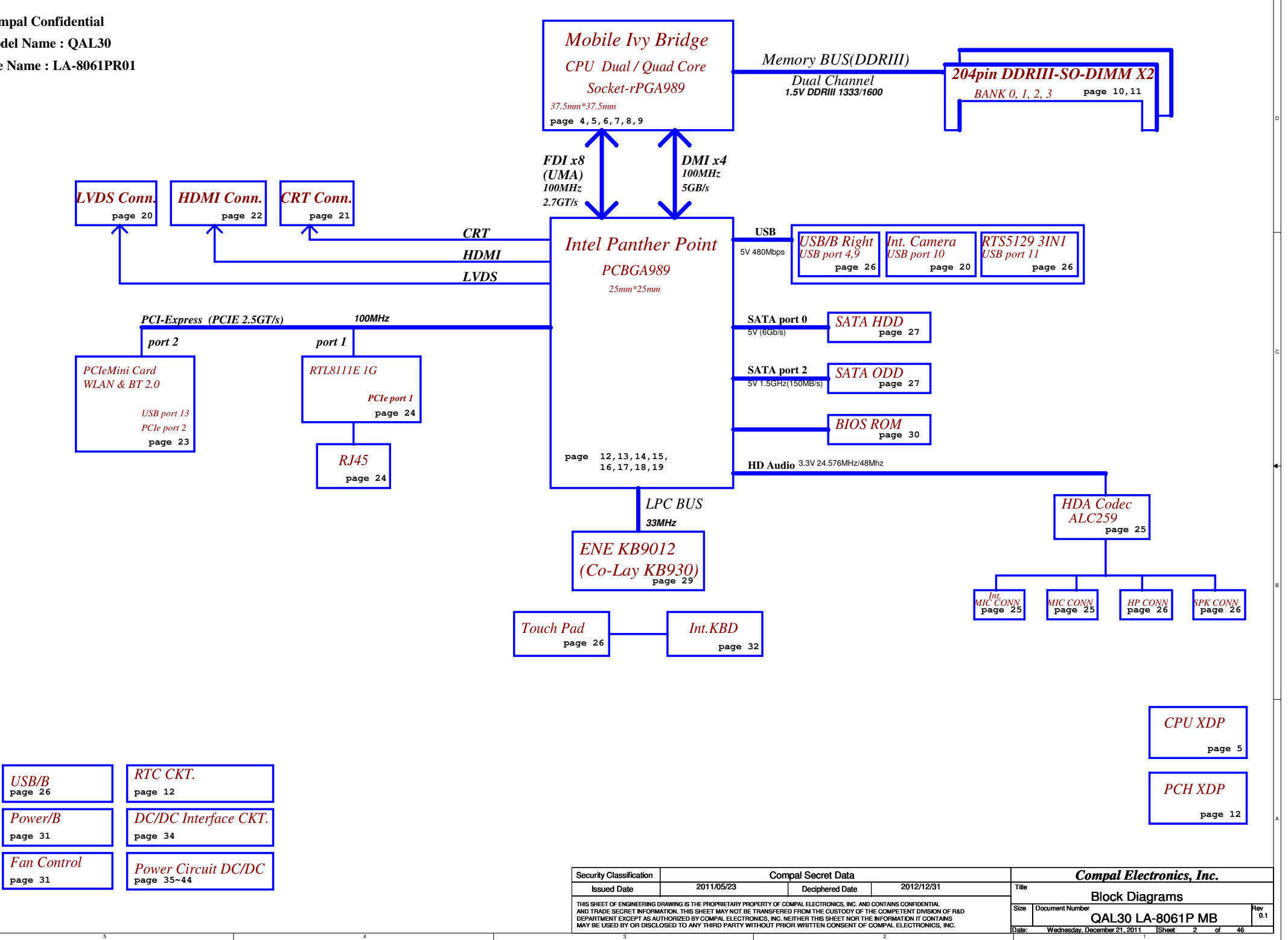
***QAL30 Project***

**LA-8061P REV 0.4 Schematic**

Intel Ivy Bridge/Panther Point

2012-01-13 Rev. 0.4

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	<b>Cover Sheet</b>
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Power Circuit DC/DC  
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CPU XDP  
page 5

PCH XDP  
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	
2	
3	
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	PCH		
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X		
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V		
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V			
PCH_SML1CLK PCH_SML1DATA	PCH	X	X	X	X			


CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None


PCH	USB PORT#	DESTINATION
	0	USB2/3 (Left Hand disc front)
	1	USB2/3 (Left Hand disc back)
	2	None
	3	None
	4	USB2 (Right Hand side front)
	5	None
	6	None
	7	None
	8	None
	9	USB2 (Left Hand side back)
	10	CAMERA
	11	Card Reader
	12	None
	13	BT Comb

OPTIMUS: XDP@/D@

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

Symbol Note :

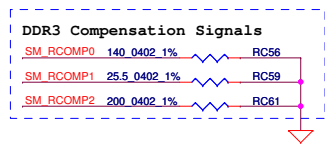
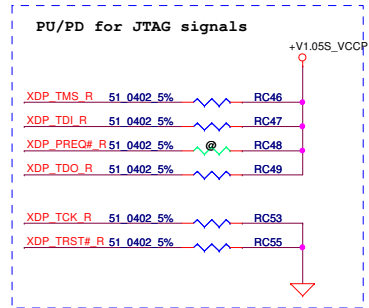
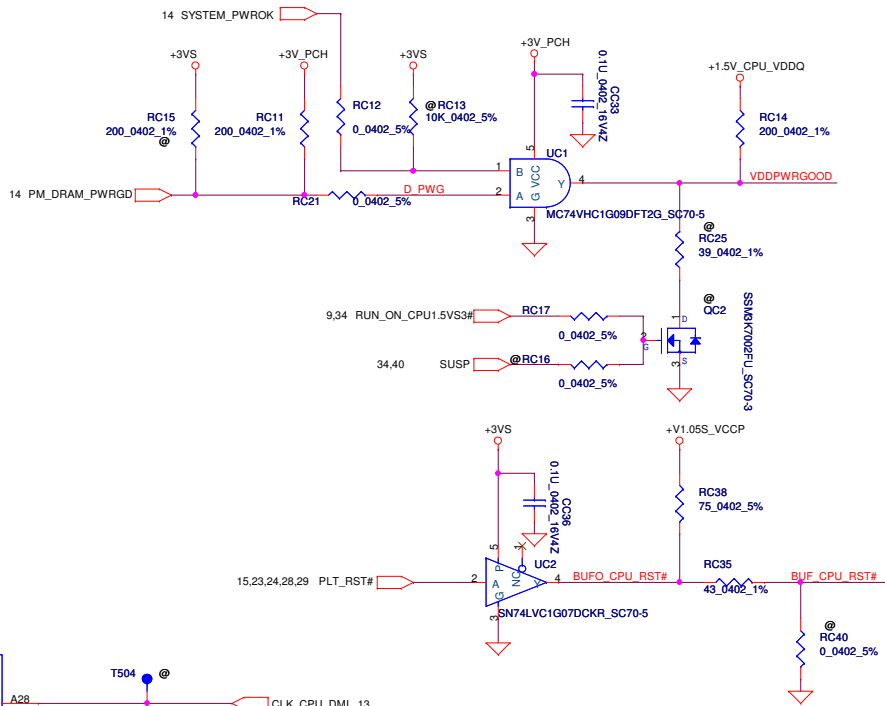
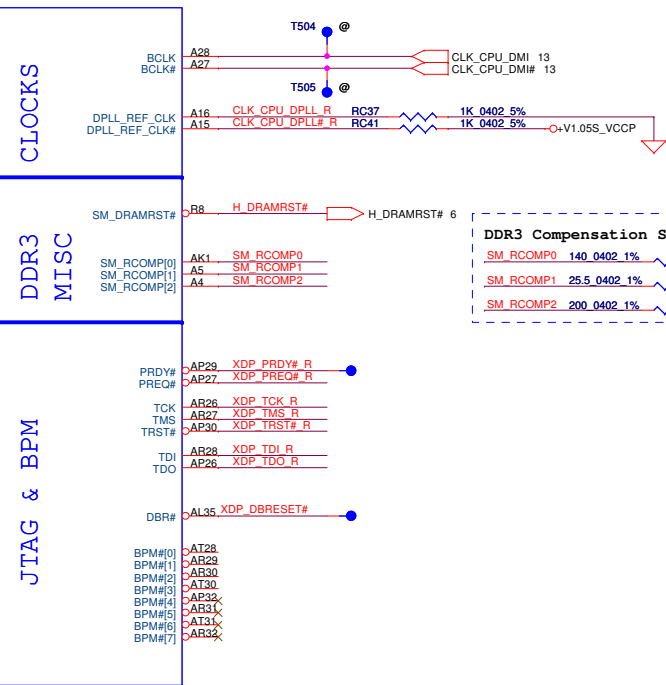
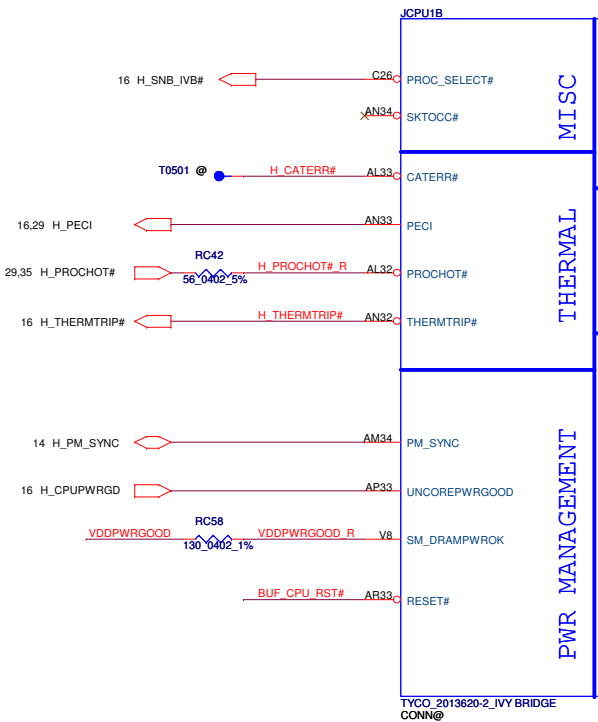
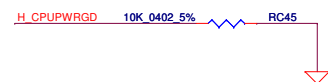
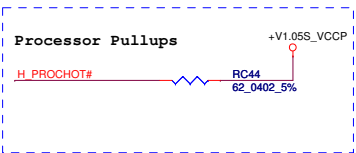
 : means Digital Ground

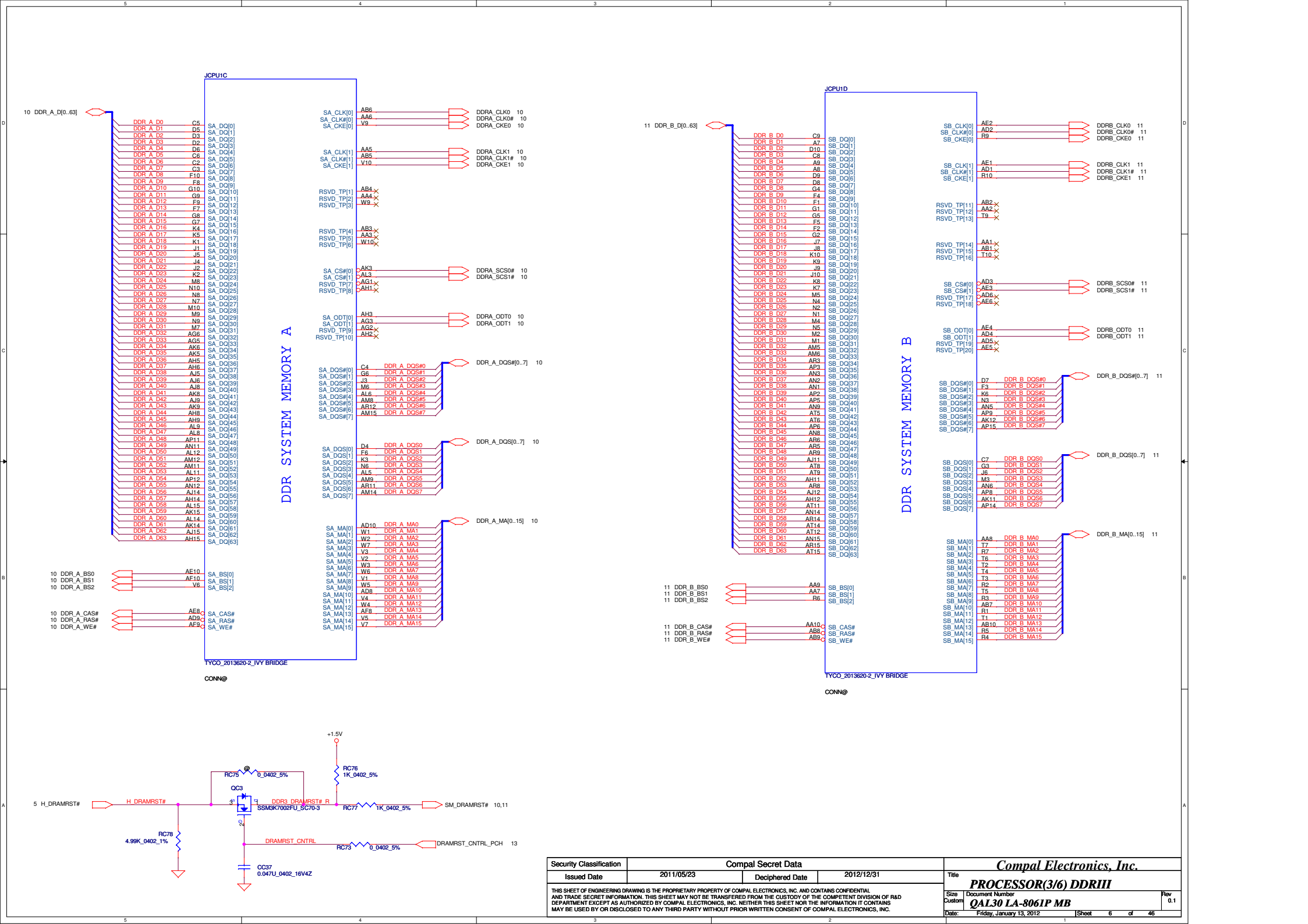
 : means Analog Ground

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

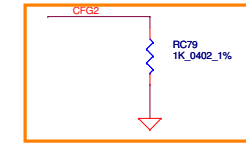
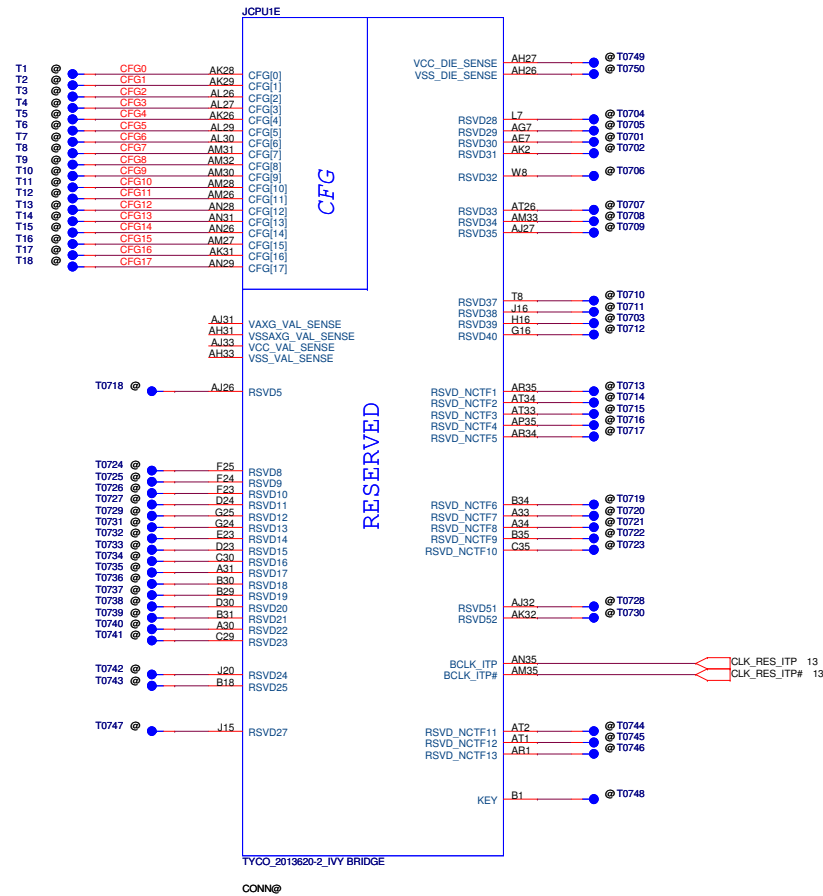
PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



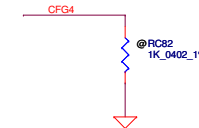




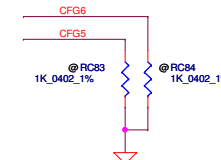
## CFG Straps for Processor



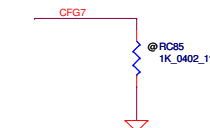
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



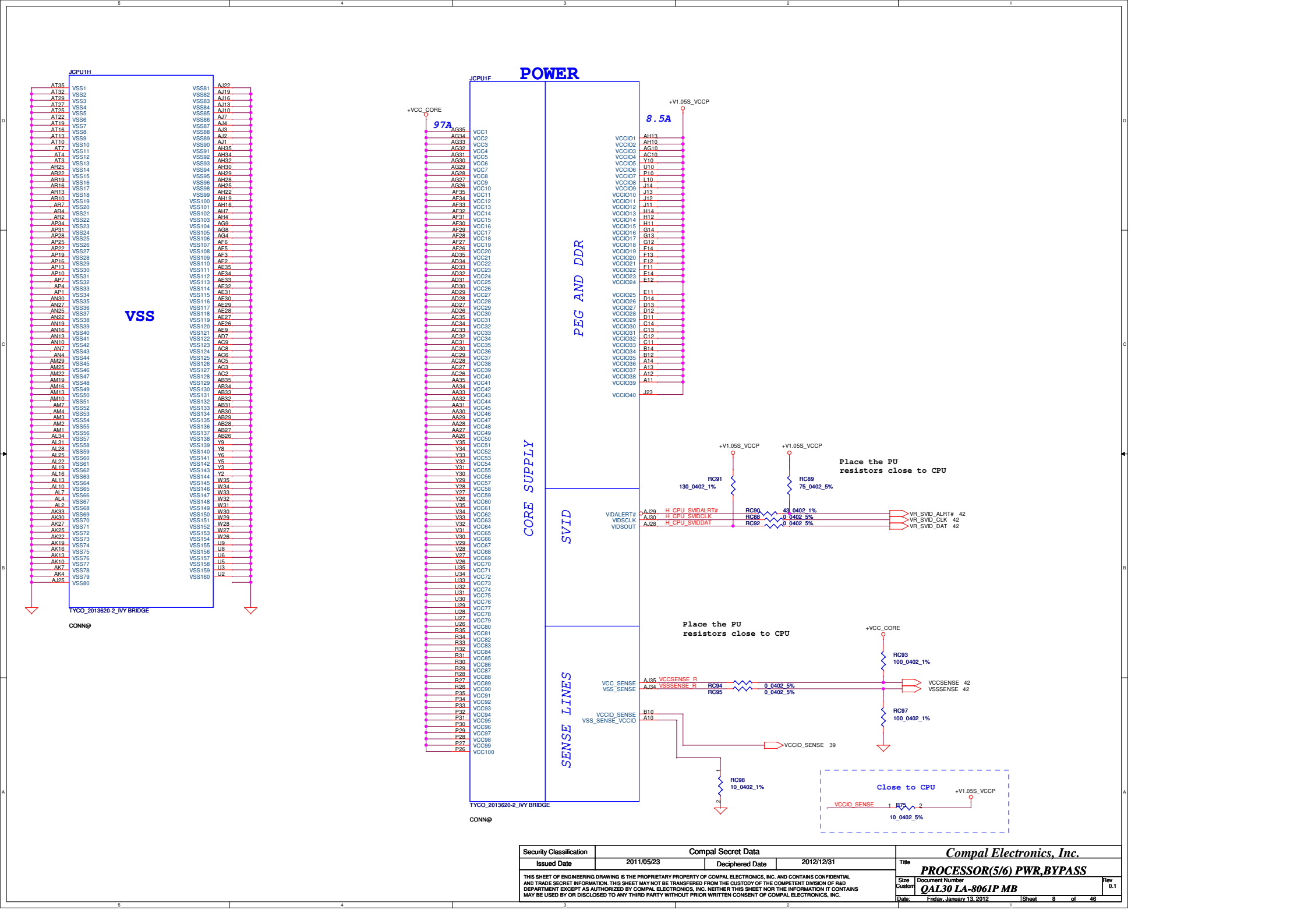
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



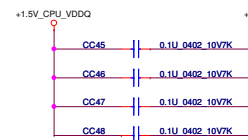
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



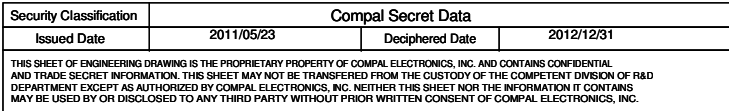
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

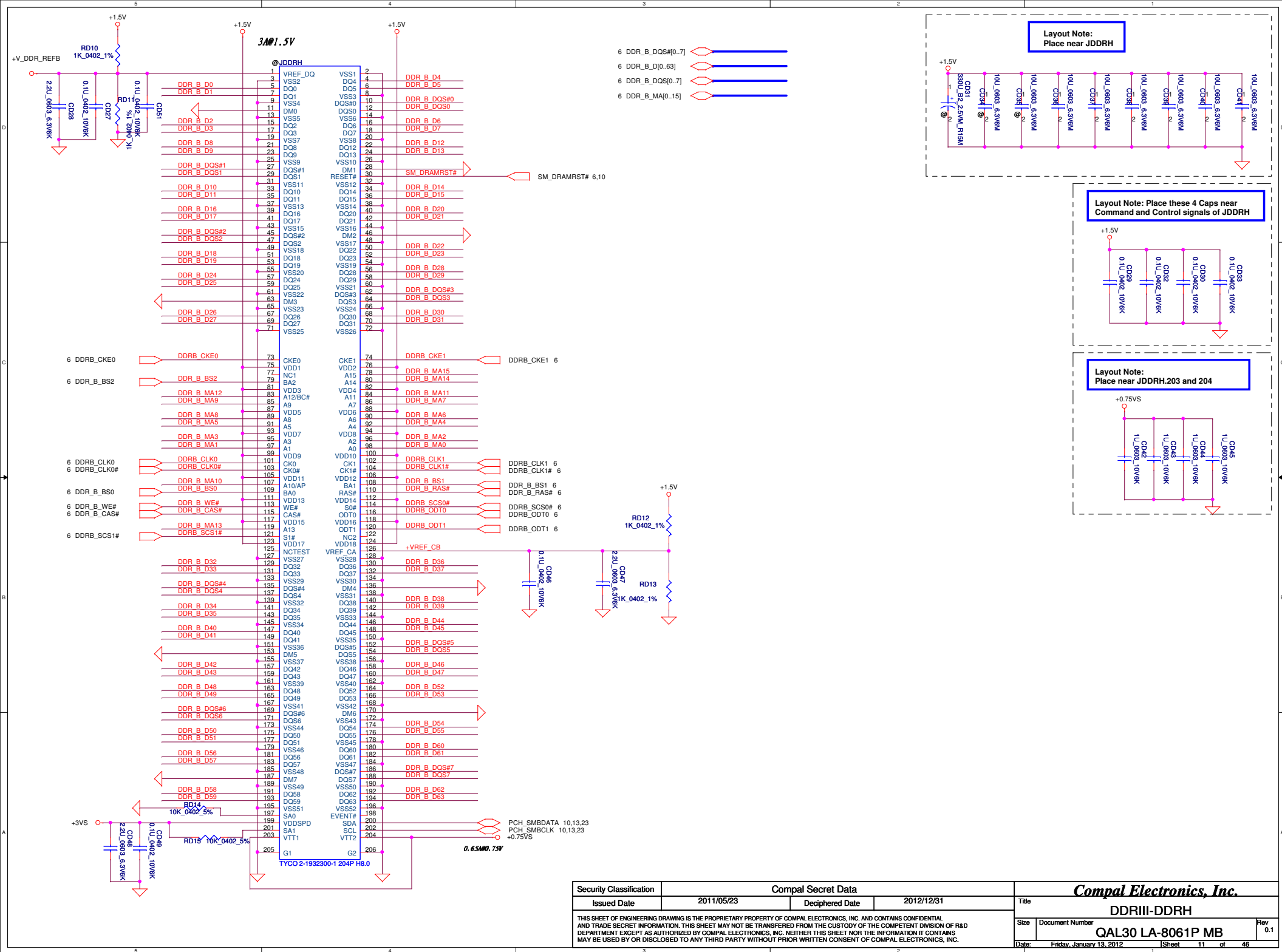






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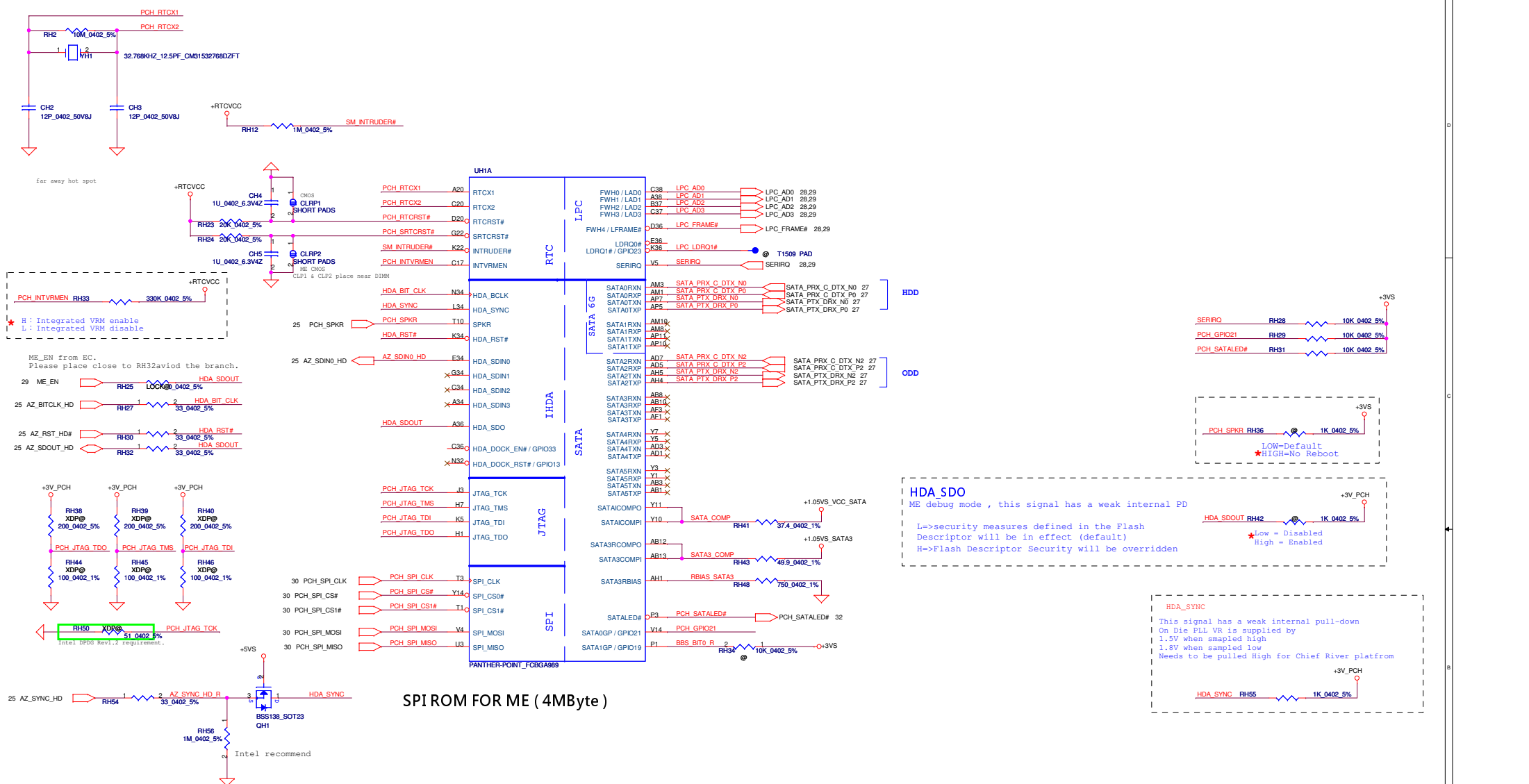


Layout Note:  
Place near JDDRH

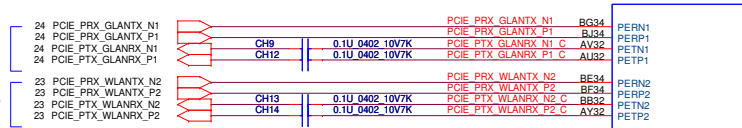
Layout Note: Place these 4 Caps near  
Command and Control signals of JDDRH

Layout Note:  
Place near JDDRH.203 and 204

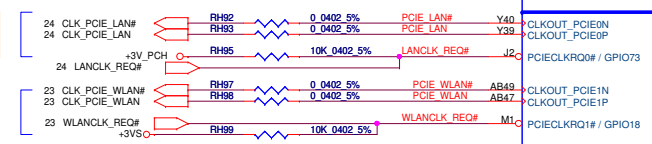
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								DDRIII-DDRH	
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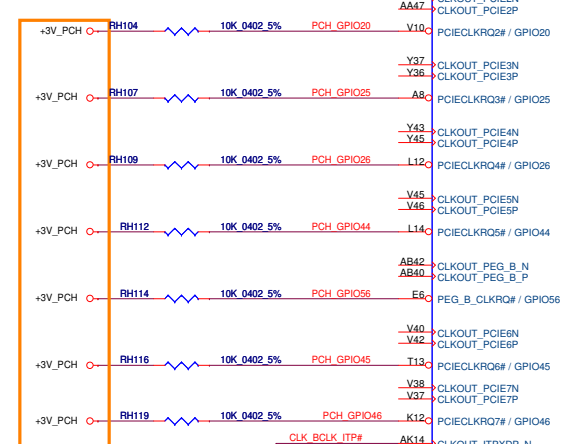
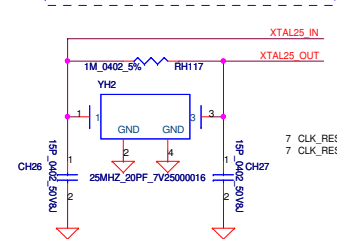
10/100/1G LAN ---->  
MiniWLAN (Mini Card 1)---->



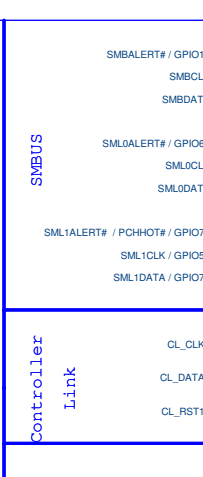
10/100/1G LAN ---->  
MiniWLAN (Mini Card 1)---->



CLK PCI LPBACK  
Reserve for EMI please close to UH4



UH1B



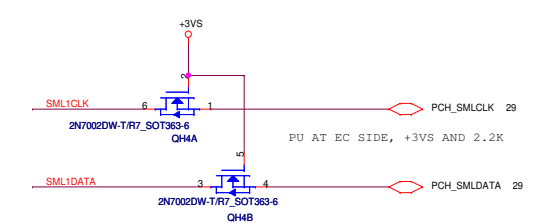
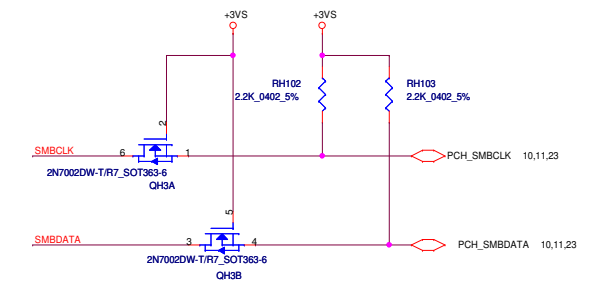
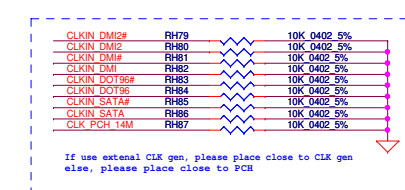
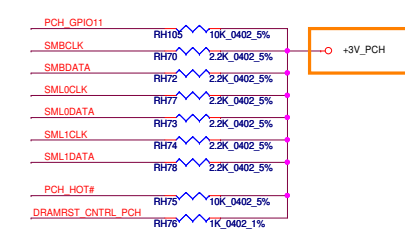
CLOCKS

FLEX CLOCKS

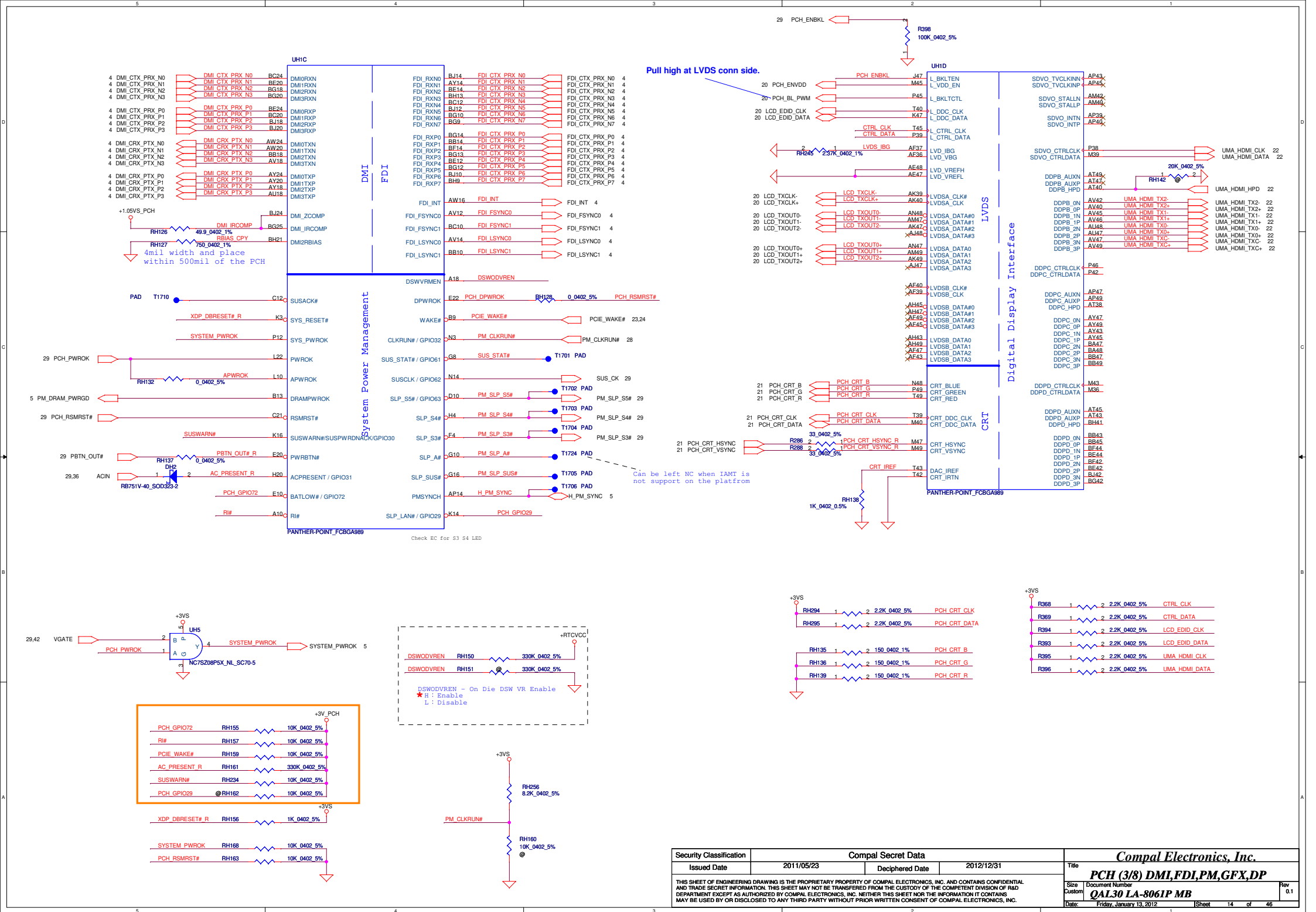
PANTHER-POINT\_FCBGA989

MEMORY

+3V\_PCH

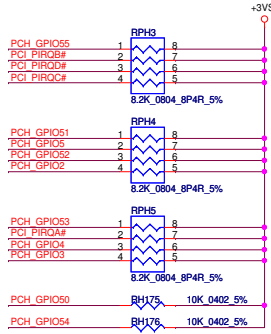
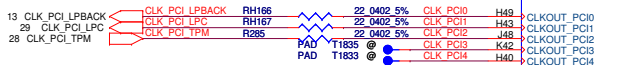
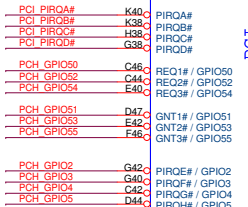
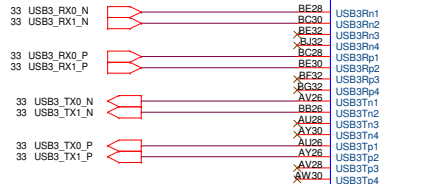


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USB3.0 Port0  
Port 0 : Left USB3.0

USB3.0 Port1  
Port 1 : Left USB3.0 with e-SATA

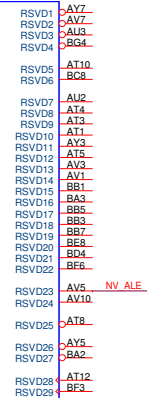


RSVD

PCI

USB

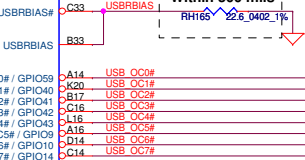
PANTHER-POINT\_FCBGA989



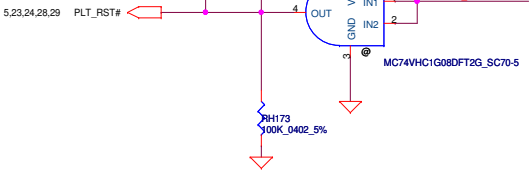
Reserved for USB3.0

USB3.0 Port0 for 2.0  
USB3.0 Port1 for 2.0  
USB3.0 Port2 for 2.0  
USB3.0 Port3 for 2.0  
Port 4 : RHS SB USB2.0

Port 9 : RHS SB USB2.0  
Port 10 : Int. Carema  
Port 11 : Card Reader  
Port 13 : BT



PLT\_RST#

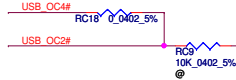
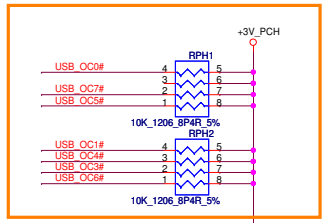


GPIO19 => BBS_BIT0		
GPIO51 => BBS_BIT1		
Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Technology	
NV_AL#	High=Enabled
	Low=Disable(floating) ★

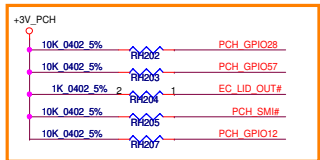
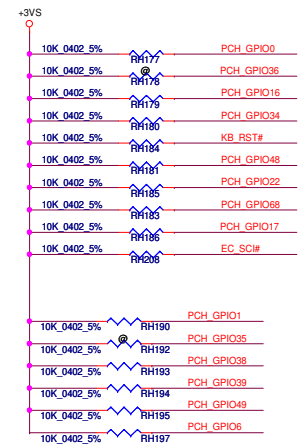
NV\_AL# @ RH164 1K 0402 5% +1.8VS

Port 0 : Left USB3.0  
Port 1 : Left USB3.0 with e-SATA

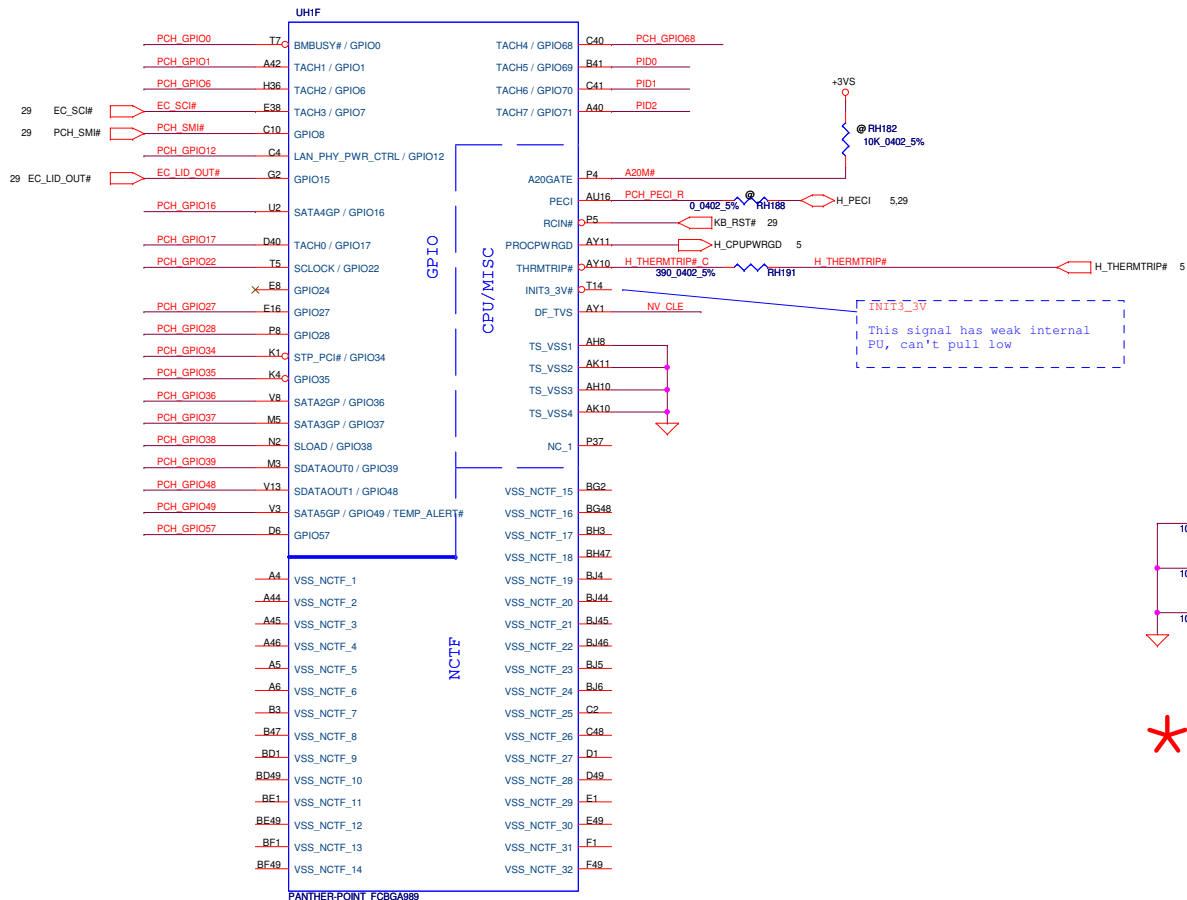
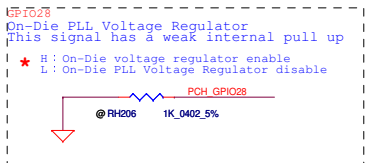


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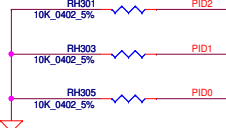
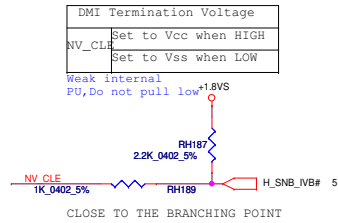




GPIO36/37  
When Unused as GPIO or SATA\*GP -  
Use 8.2K-10K pull-down to ground.



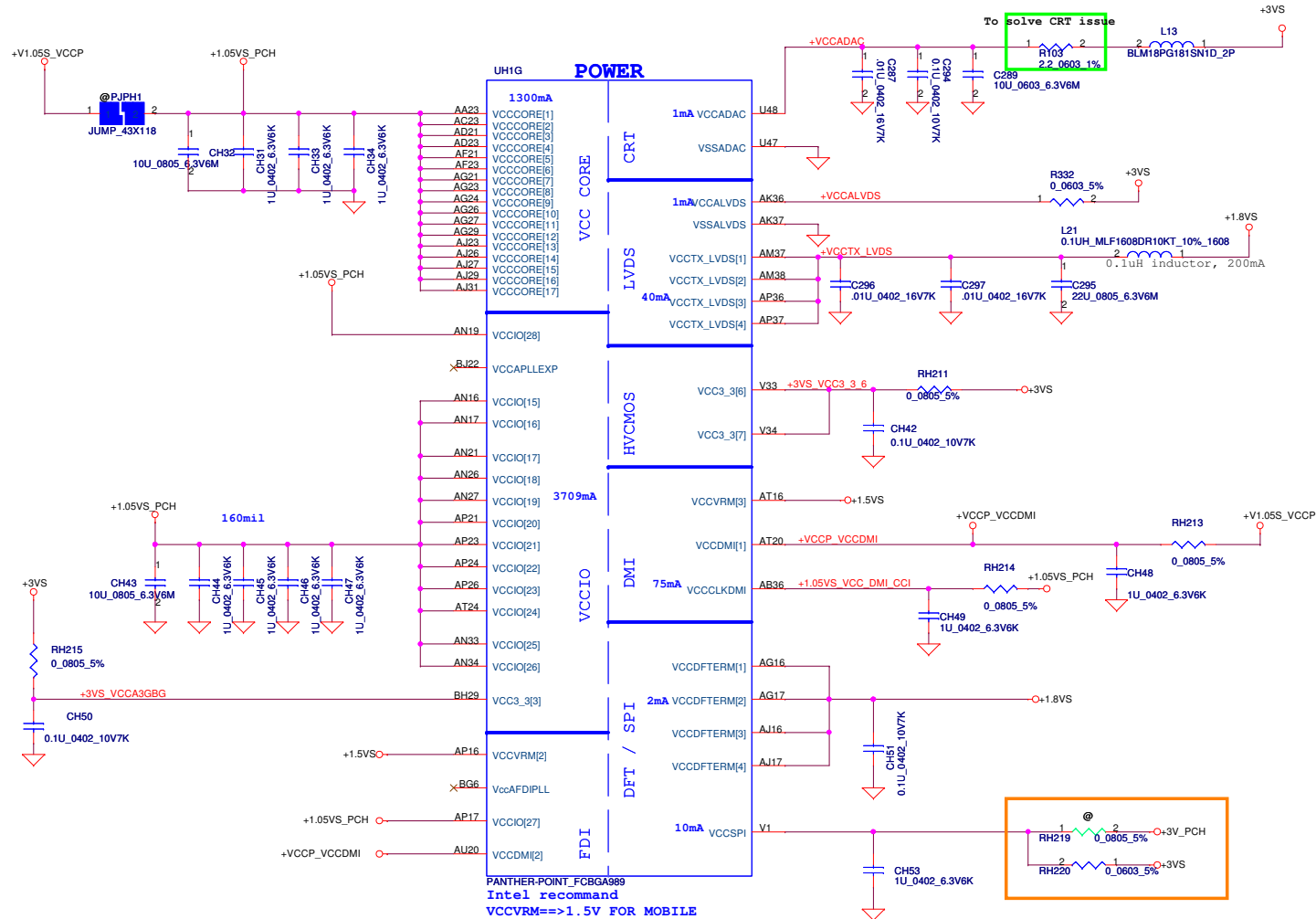
PCH\_GPIO28 needs to be connected to XDP\_FN8  
PCH\_GPIO35 needs to be connected to XDP\_FN9  
PCH\_GPIO15 needs to be connected to XDP\_FN16  
Please refer to Huron River Debug Board DG 1.2



PID :	210	
QAL30	000	(UMA)
QAL31	001	(DIS)
QAL50	010	(UMA)
QAL51	011	(DIS)
KSPD		
Q0000	1XX	

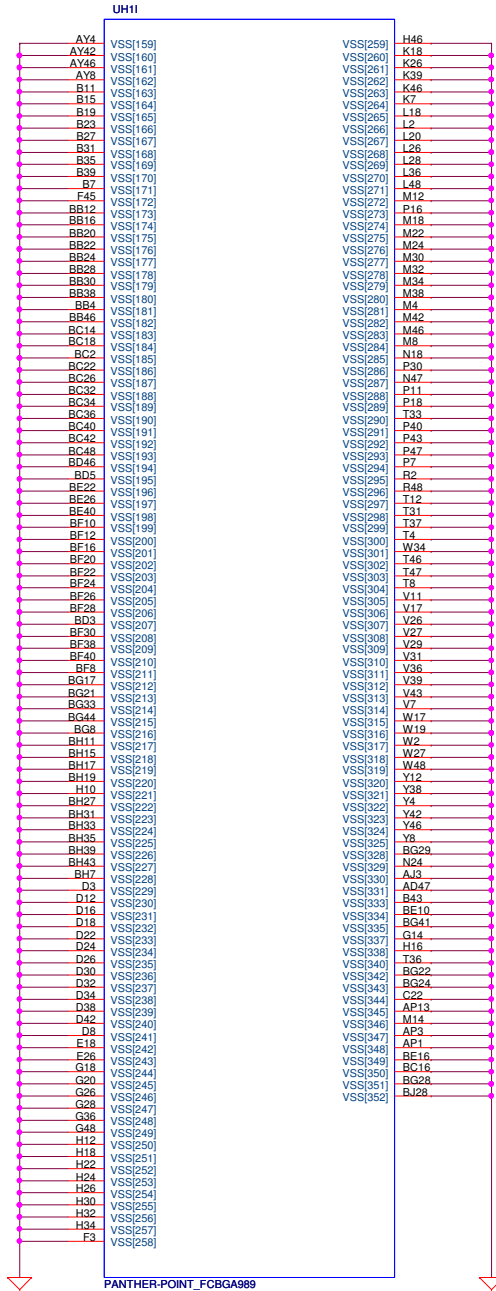
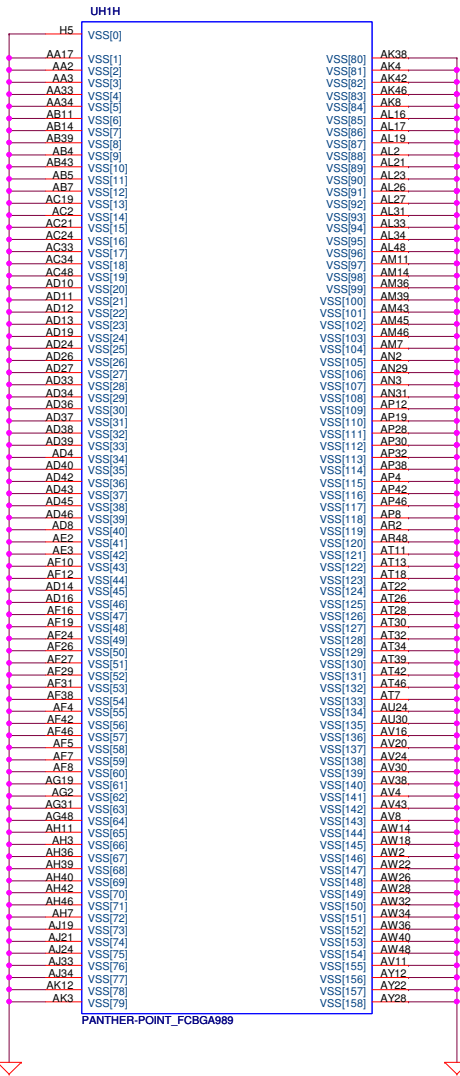
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PCH (5/8) GPIO, CPU, MISC				Rev 0.1
QAL30 LA-8061P MB				Rev 0.1
Date: Friday, January 13, 2012				Rev 0.1



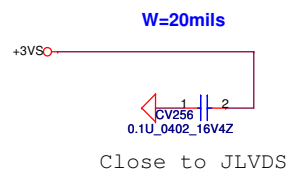
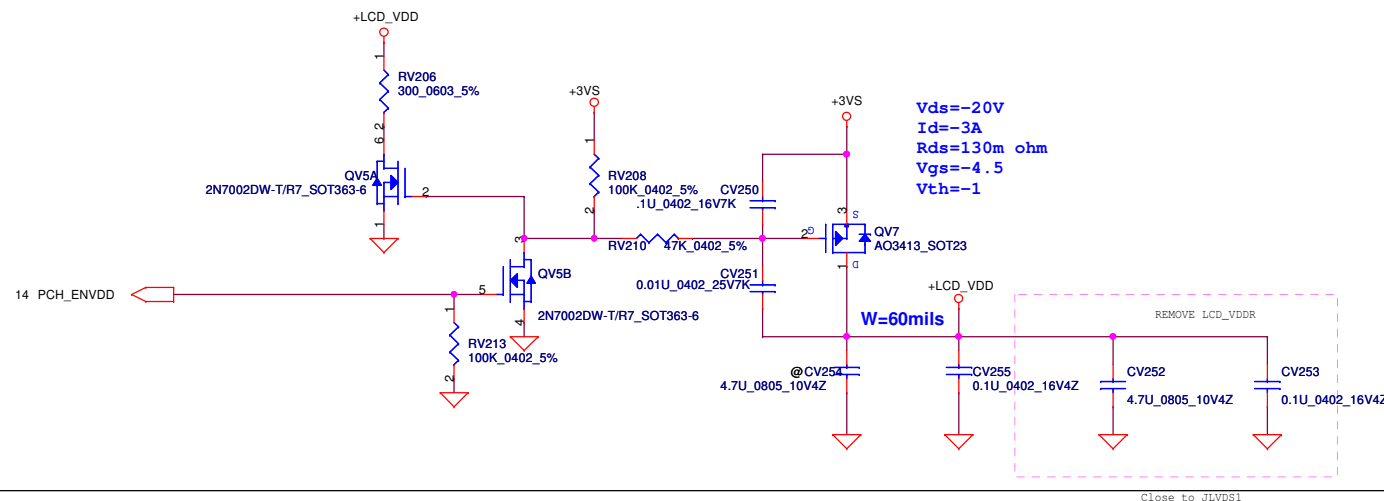
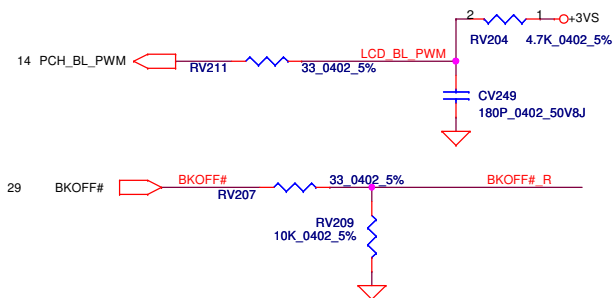


PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



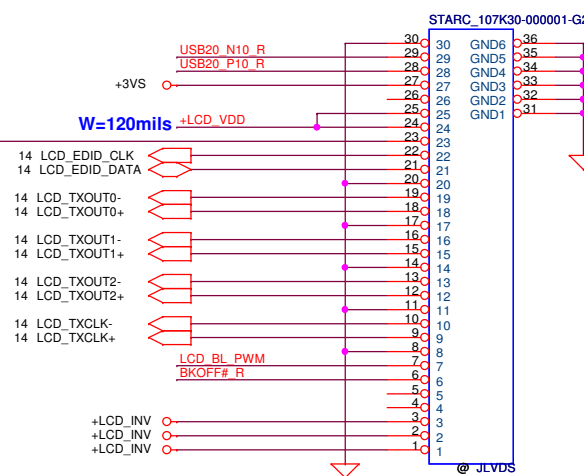
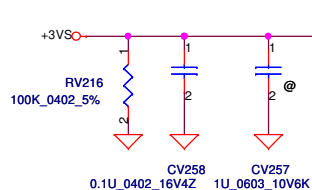


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					<b>PCH (3/8) VSS</b>
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		Date: Friday, October 26, 2011		Sheet 19	of 46

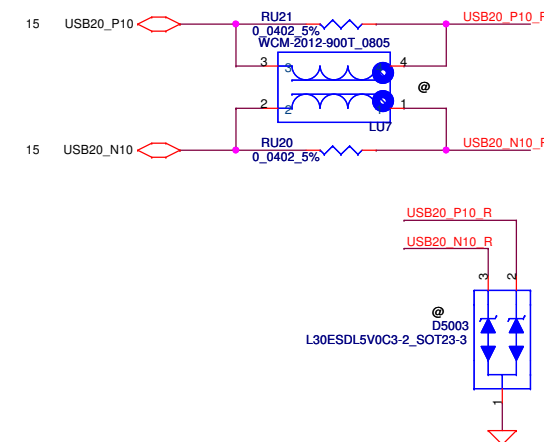
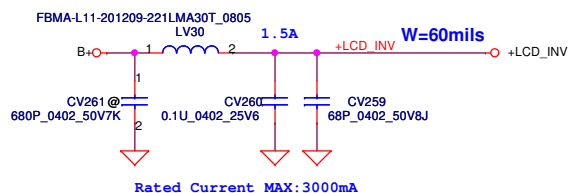


Change to 30 pin.

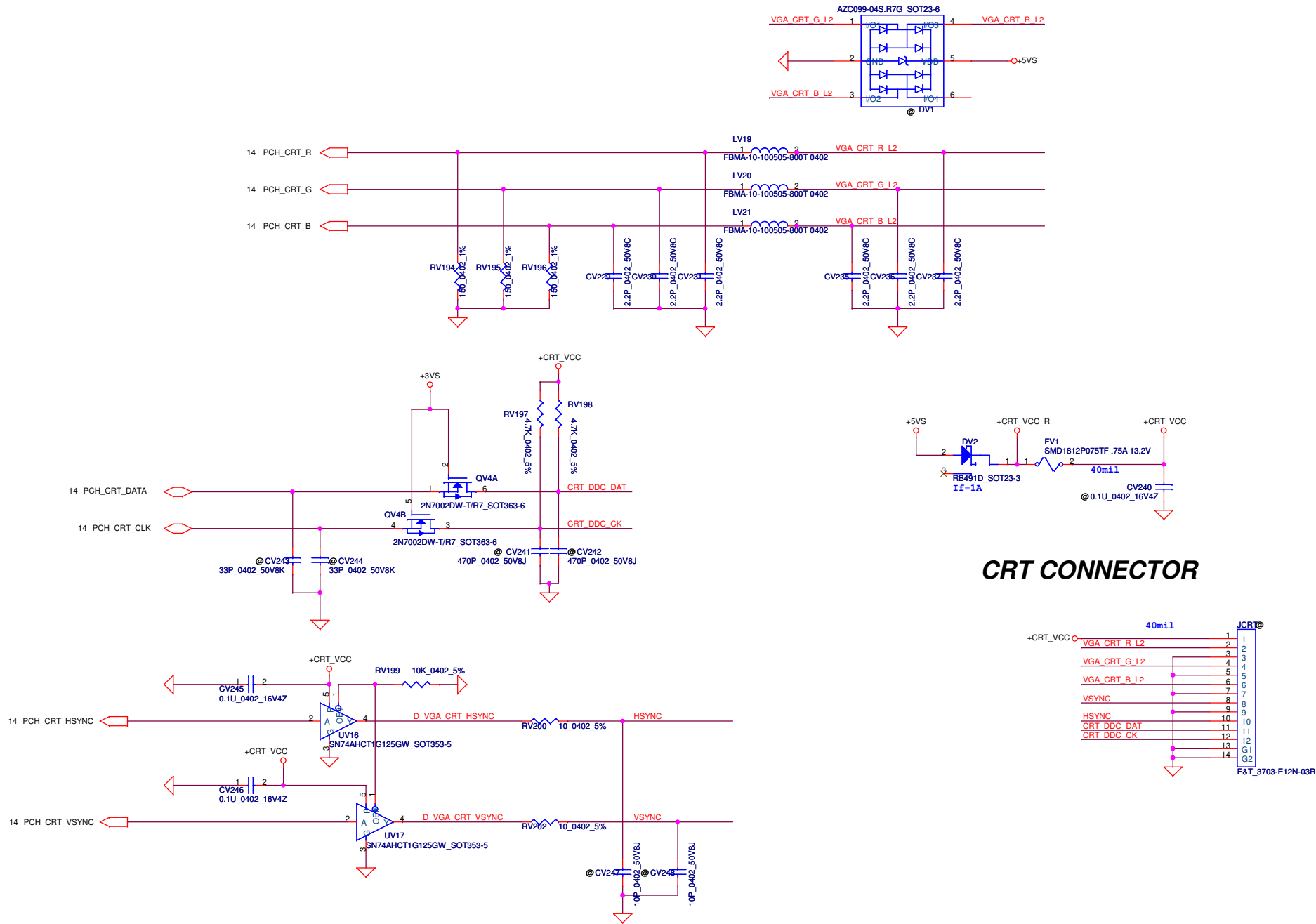
## Single Channel LVDS



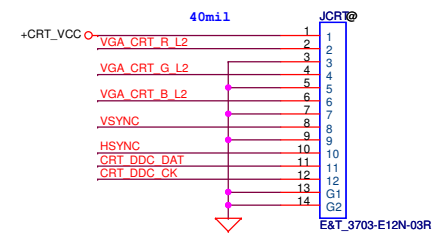
## LCD/PANEL BD. Conn.



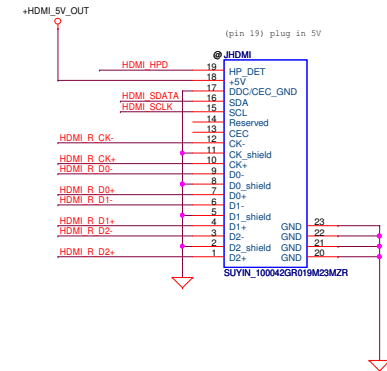
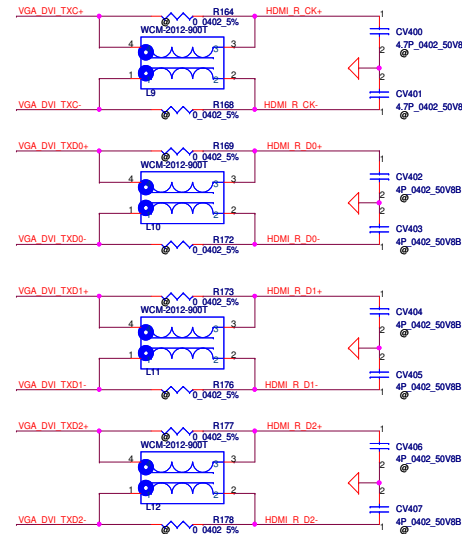
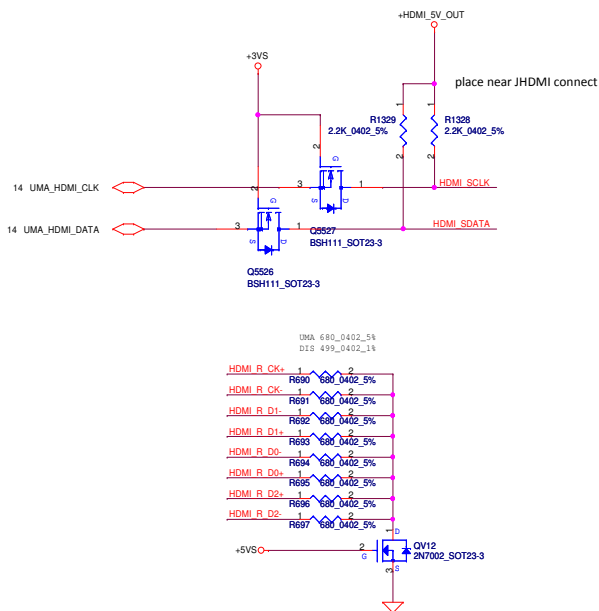
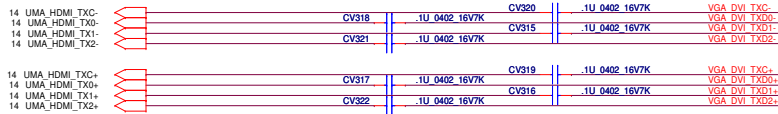
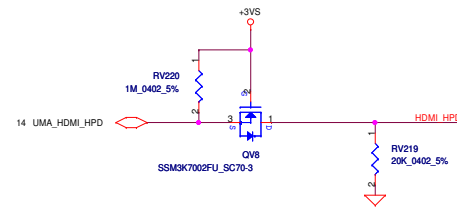
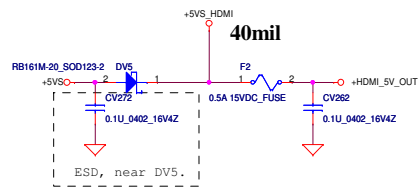
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	LVDS
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## CRT CONNECTOR

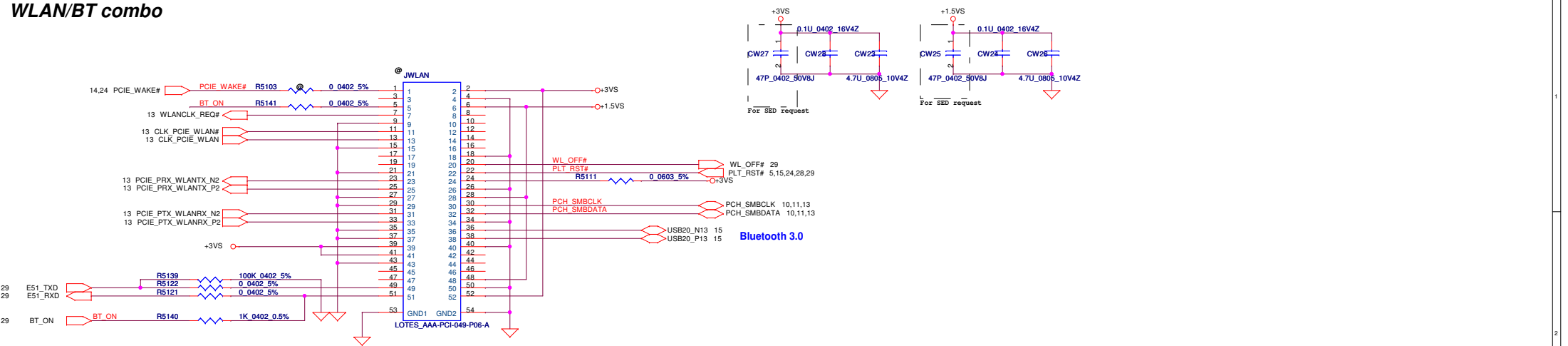


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				QAL30 LA-8061P MB	
				Date	Friday, January 13, 2012
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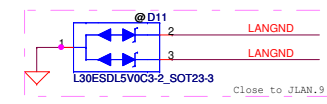
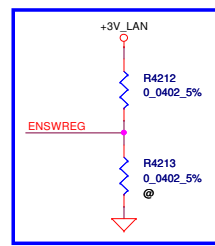
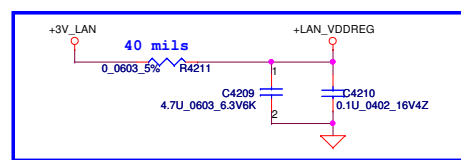
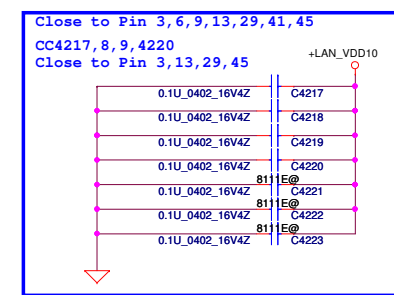
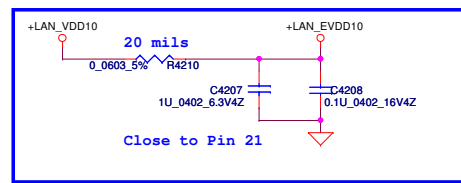
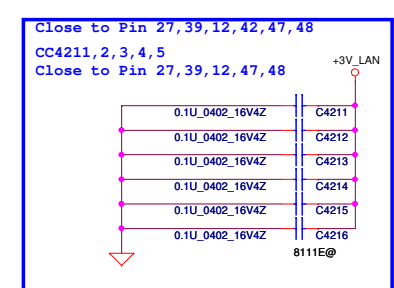
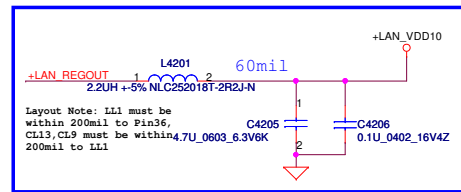
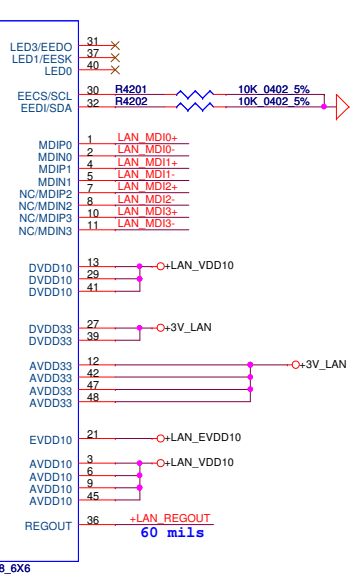
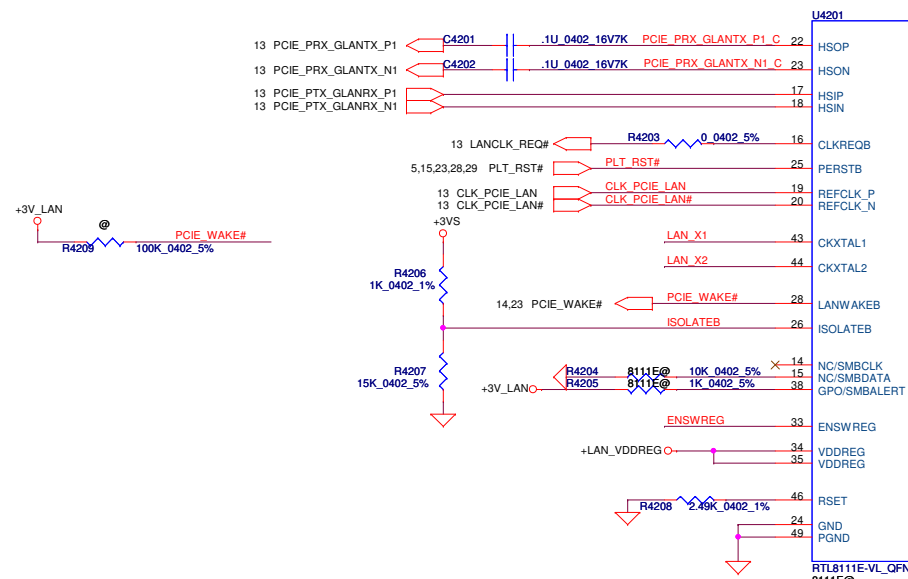


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Date: Friday, January 13, 2012				0.1
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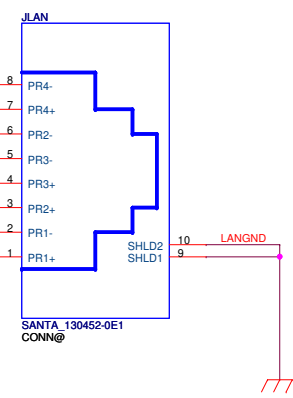
WLAN/BT combo



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				Size Custom	Document Number QAL30 LA-8061P MB	Rev 0.1
				Date: Friday, January 13, 2012	Sheet 23	of 46

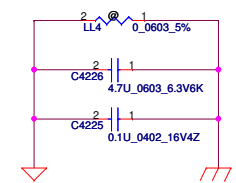
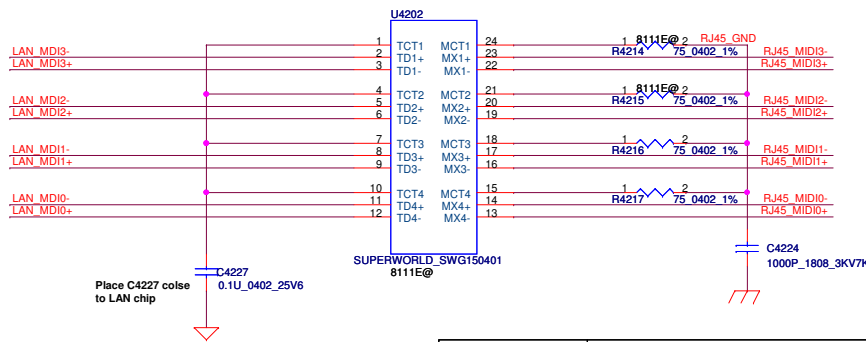
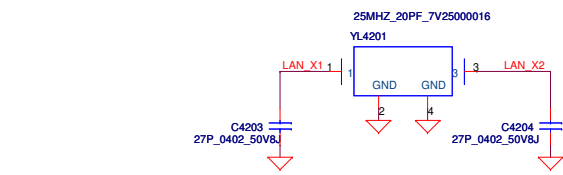
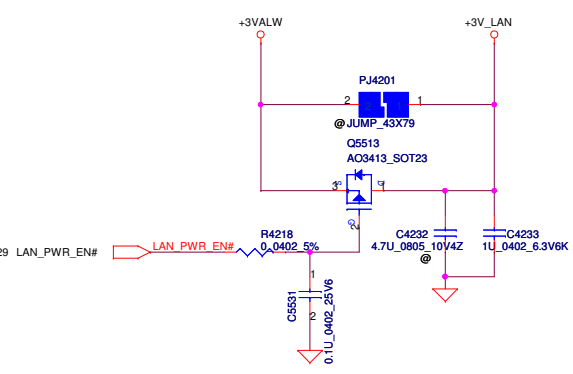


### LAN Conn.



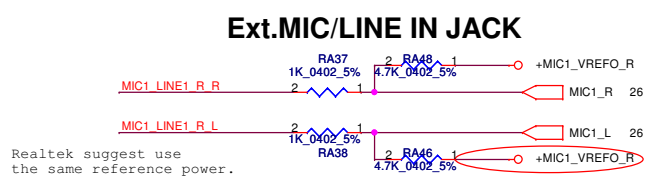
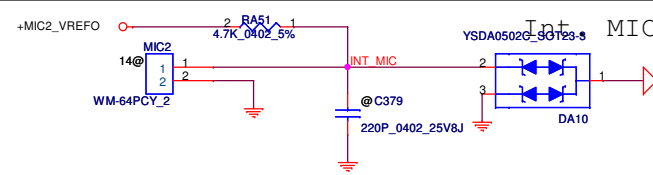
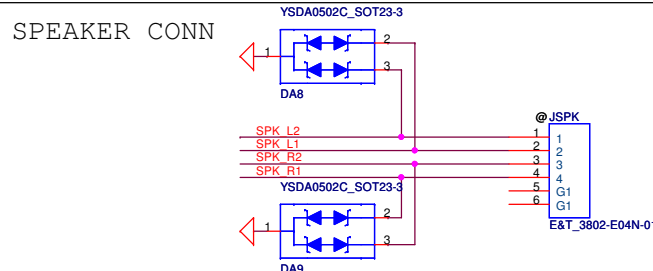
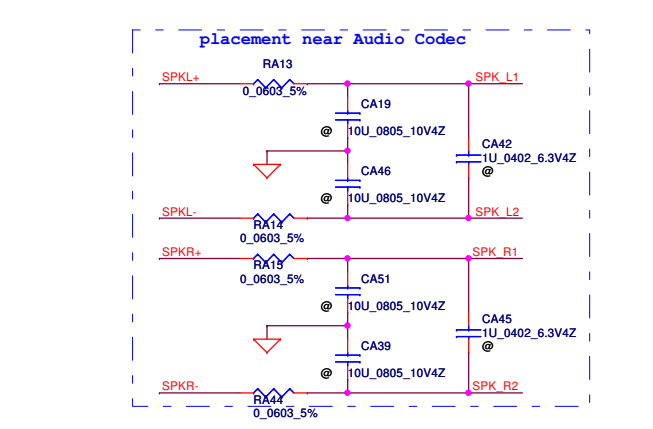
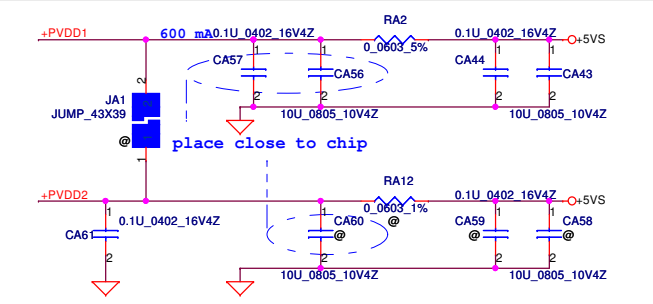
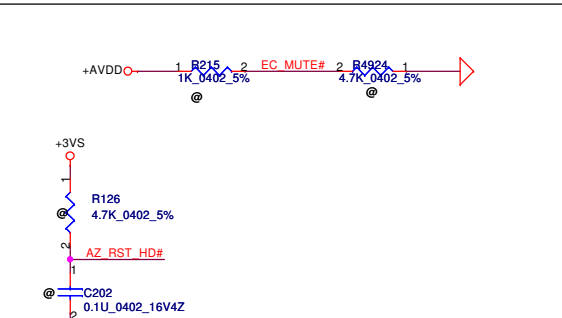
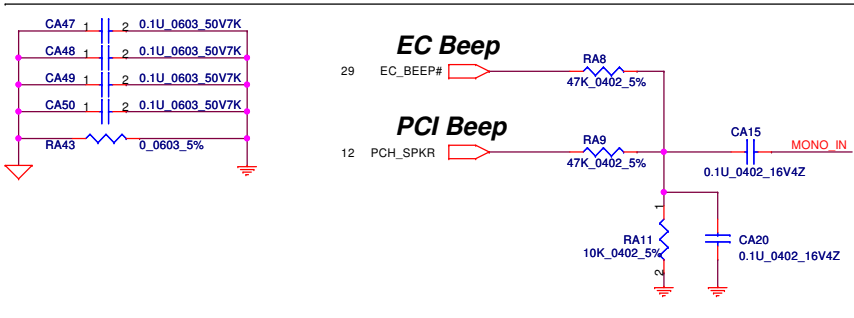
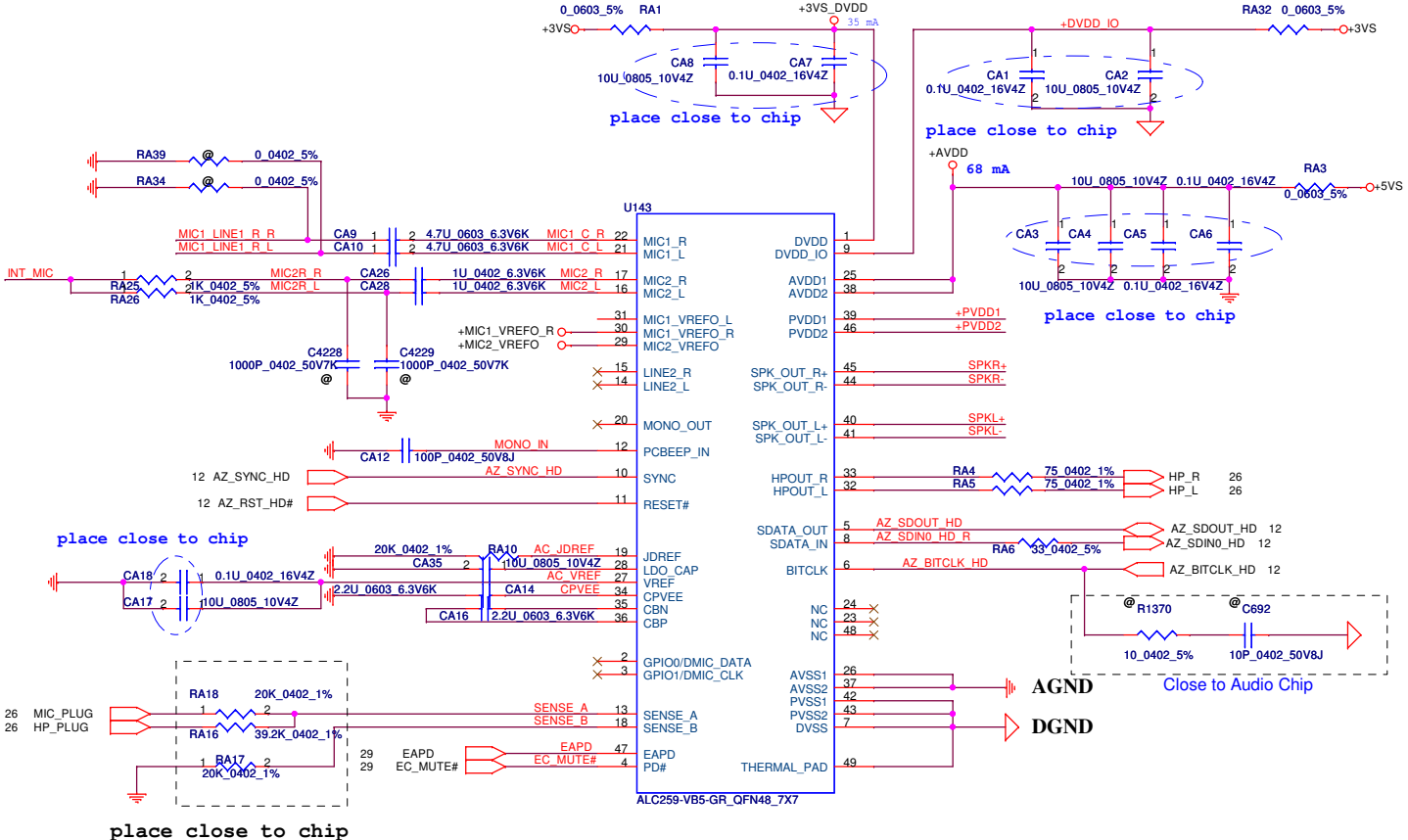
+3V\_Lan Rise time(10%~90%)要>1ms and <100ms

### +3VALW TO +3V\_LAN



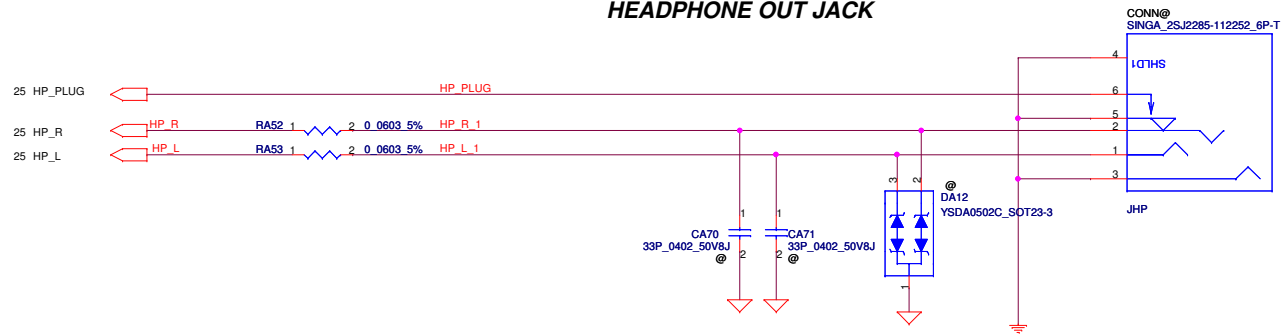
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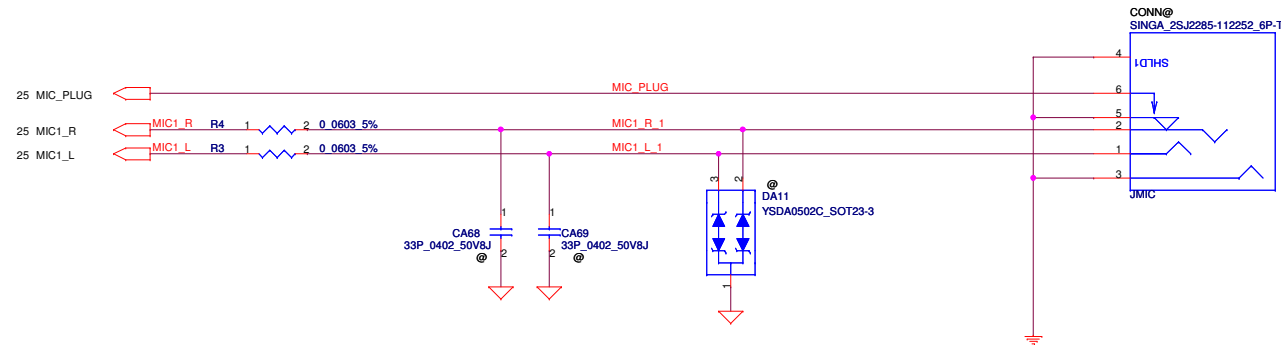


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

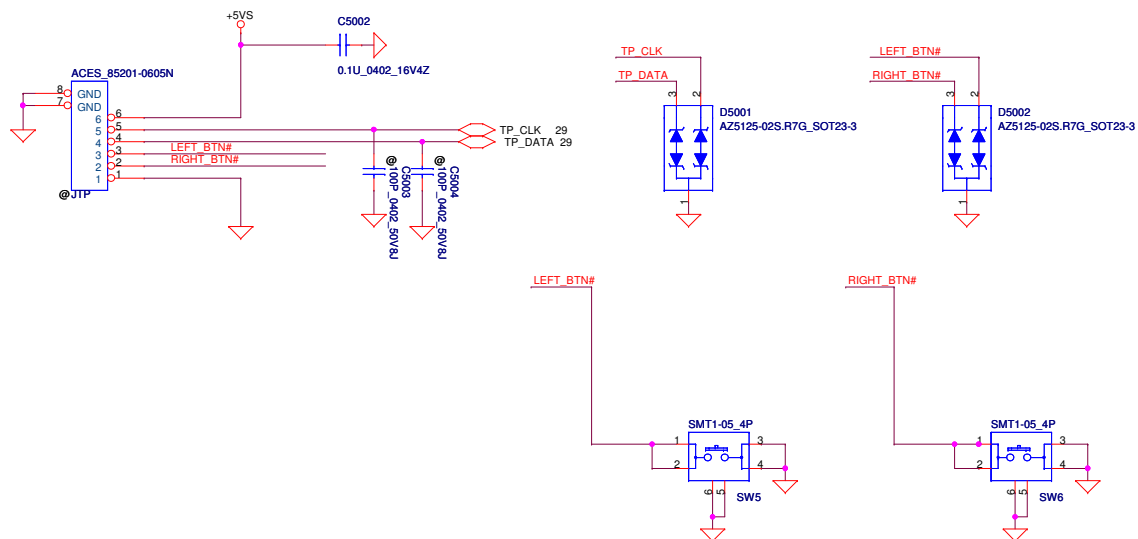
## HEADPHONE OUT JACK



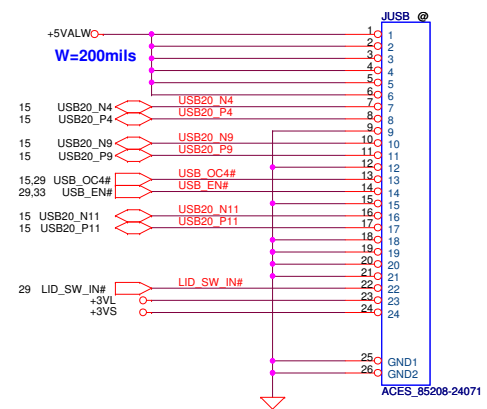
## MICROPHONE IN JACK



## Touch/B Connector

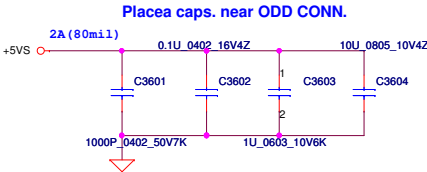
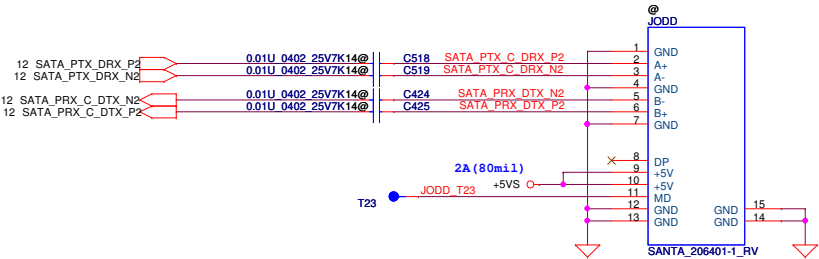


## USB + LID SB

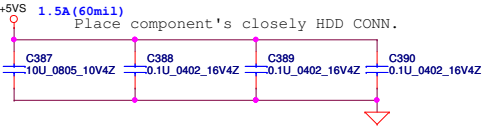
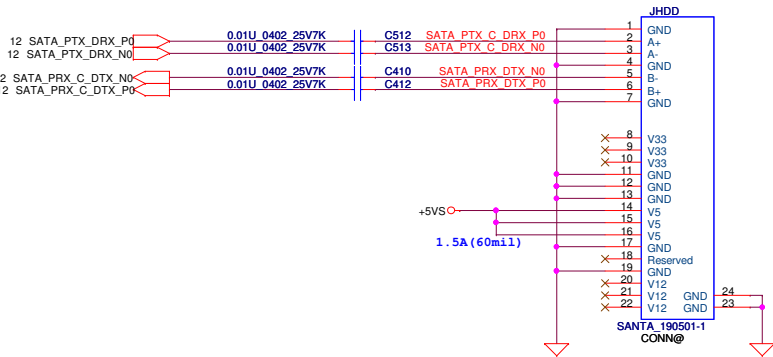


Title			
AUDIO CONN/TP/FUNB			
Size	Document Number	QAL30 LA-8061P MB	
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SATA ODD Conn.

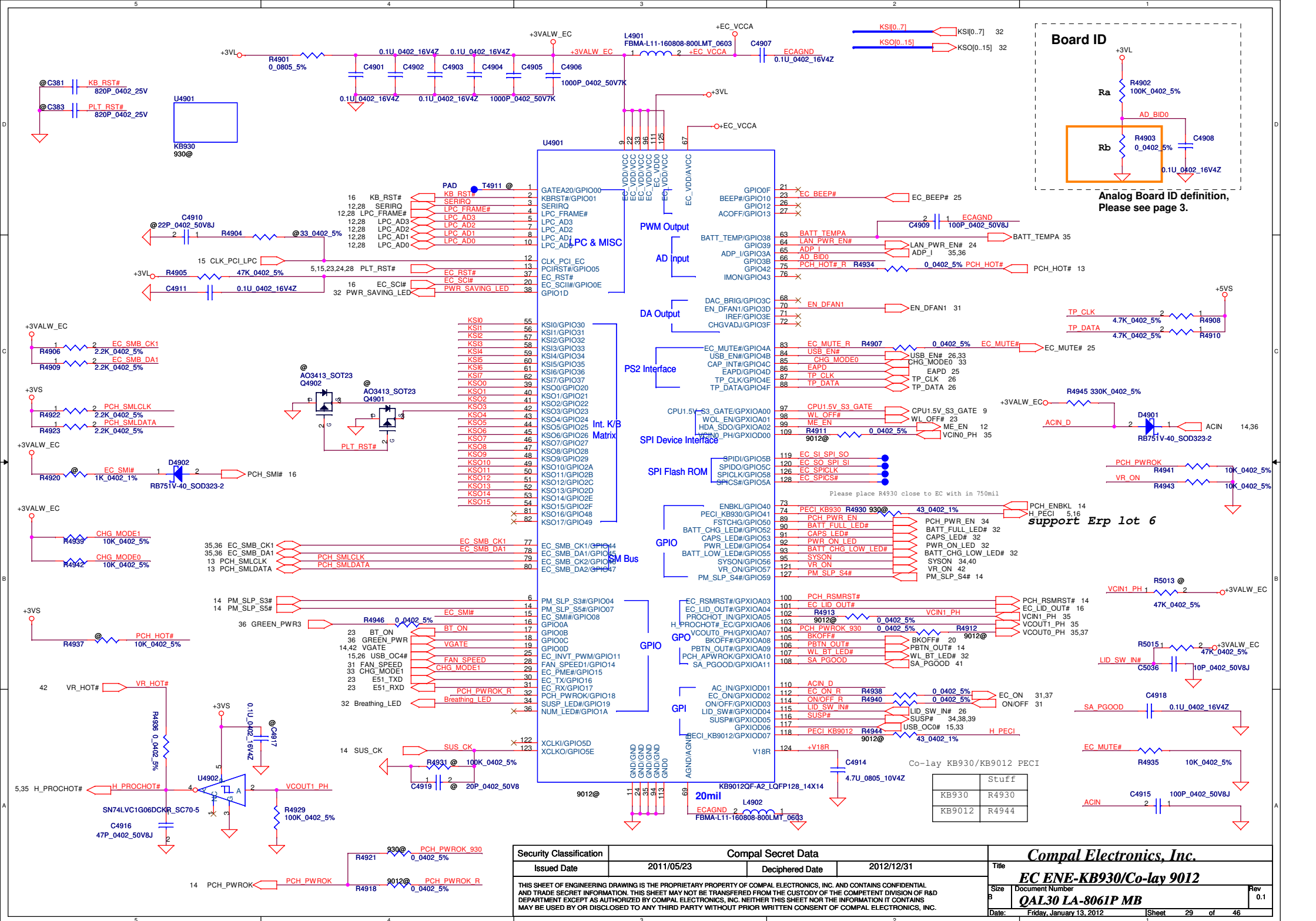


SATA HDD Conn.



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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	<b>SATA HDD / ODD</b>	
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BIOS Bus switch

R401

0.0402\_5%

NOW8@

R402

0.0402\_5%

NOW8@

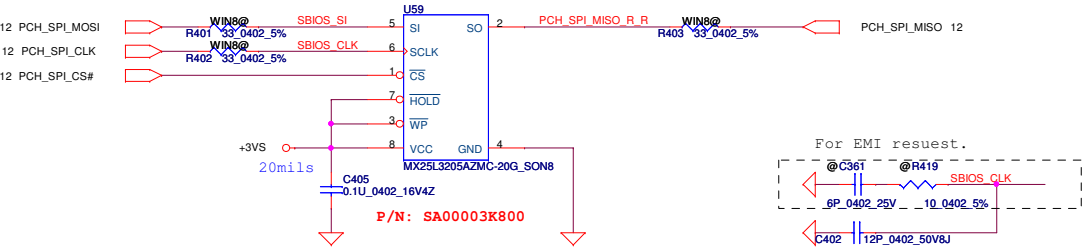
R403

0.0402\_5%

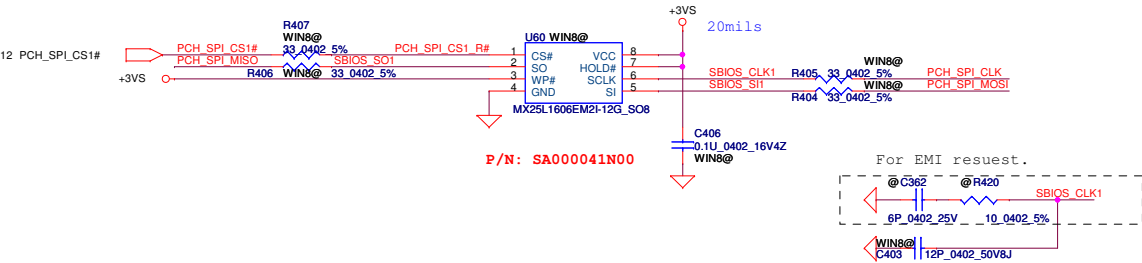
NOW8@

When use single ROM, use 0 ohm.

BIOS SPI Flash (4MByte\*1)



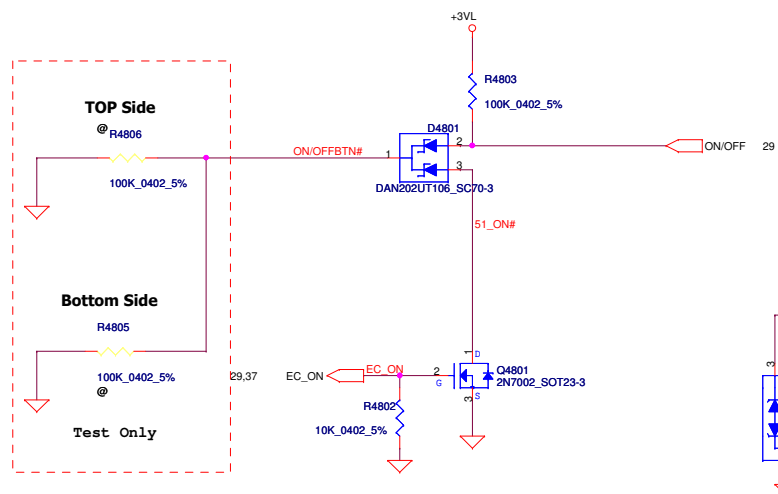
BIOS SPI Flash (2MByte\*1) For Win8



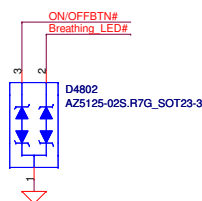
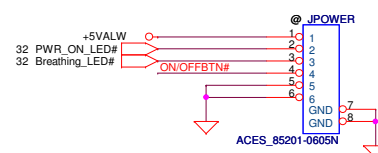
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Issued Date		Deciphered Date		SBIOS & EC ROM	
2011/05/23		2012/12/31		Size	
2011/05/23		2012/12/31		Document Number	
2011/05/23		2012/12/31		QAL30 LA-8061P MB	
2011/05/23		2012/12/31		Rev	
2011/05/23		2012/12/31		0.1	
2011/05/23		2012/12/31		Date: Friday, January 13, 2012	
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## Power Button

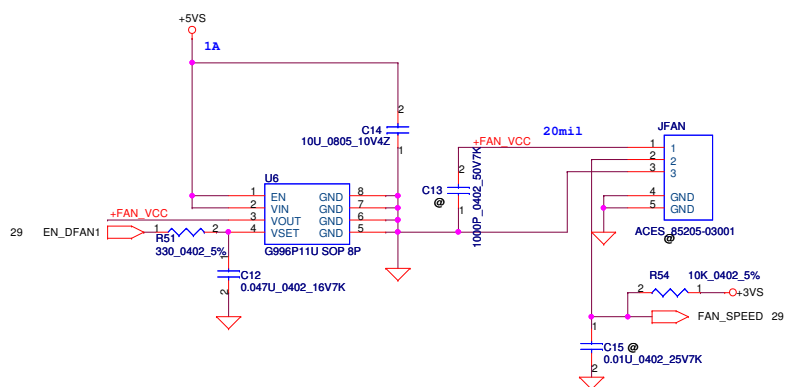
ON/OFF switch



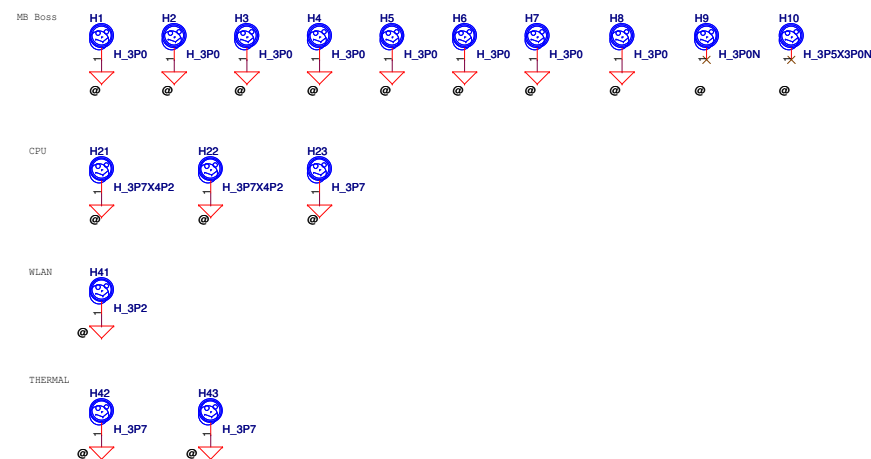
***To POWER/B***



### Fan Control Circuit



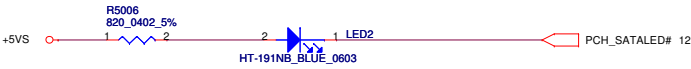
## Screw Hole



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LED

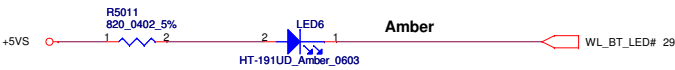
SATA



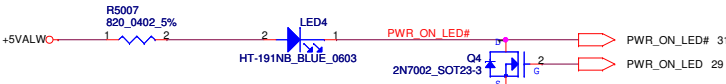
Battery



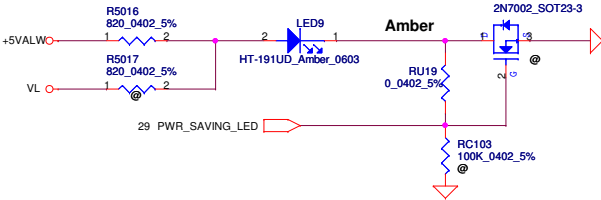
Wireless



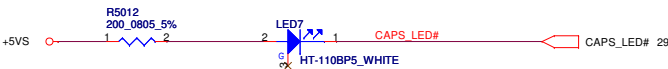
Power



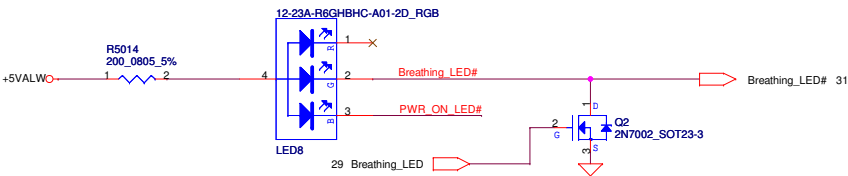
Power Saving



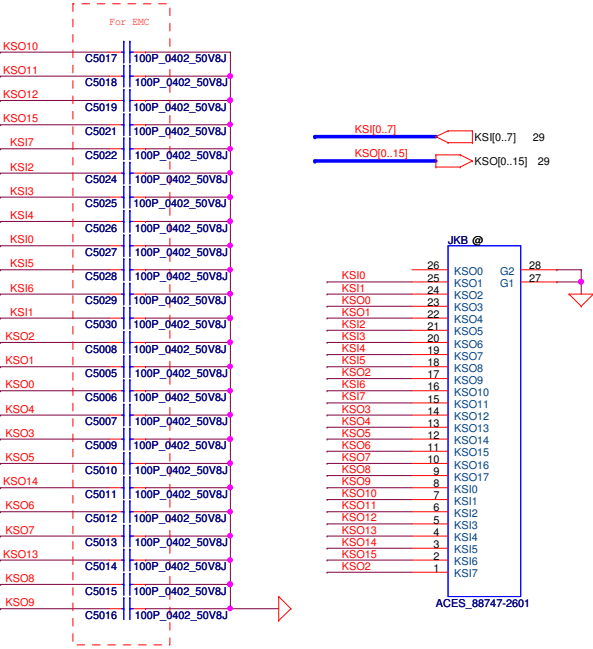
CAP Lock



Breathing



INT\_KBD Conn.

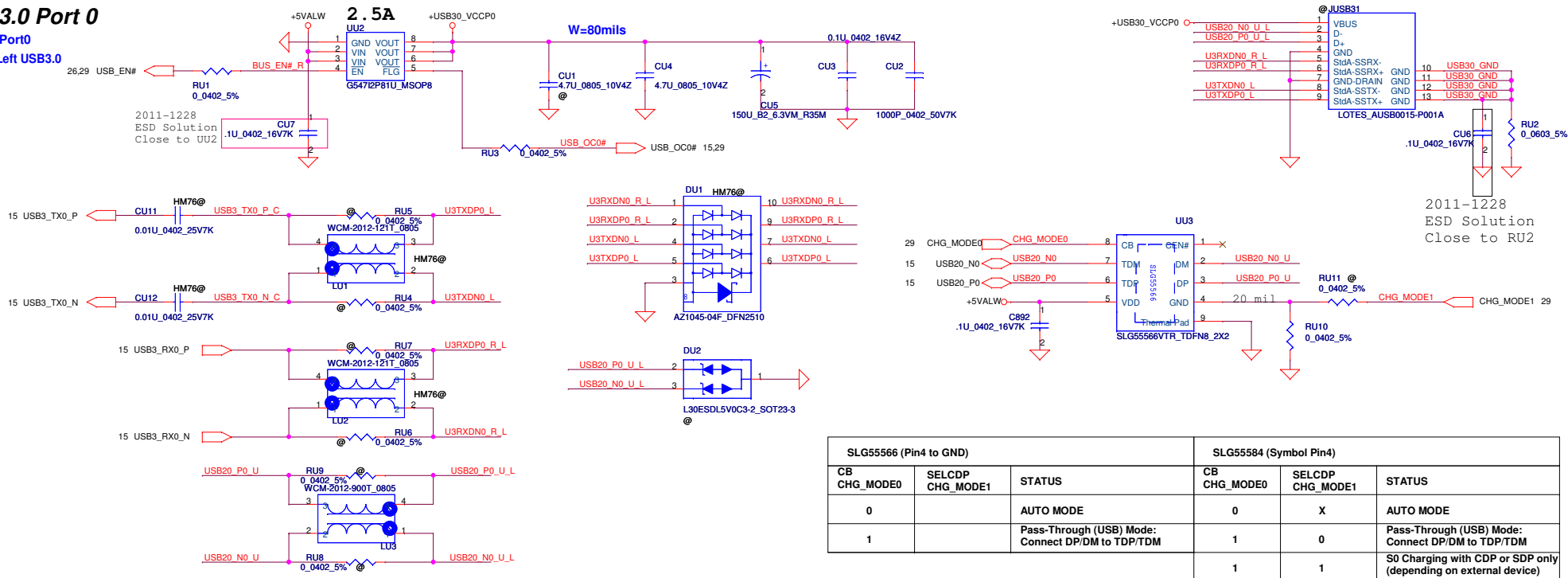




## USB3.0 Port 0

USB3.0 Port0

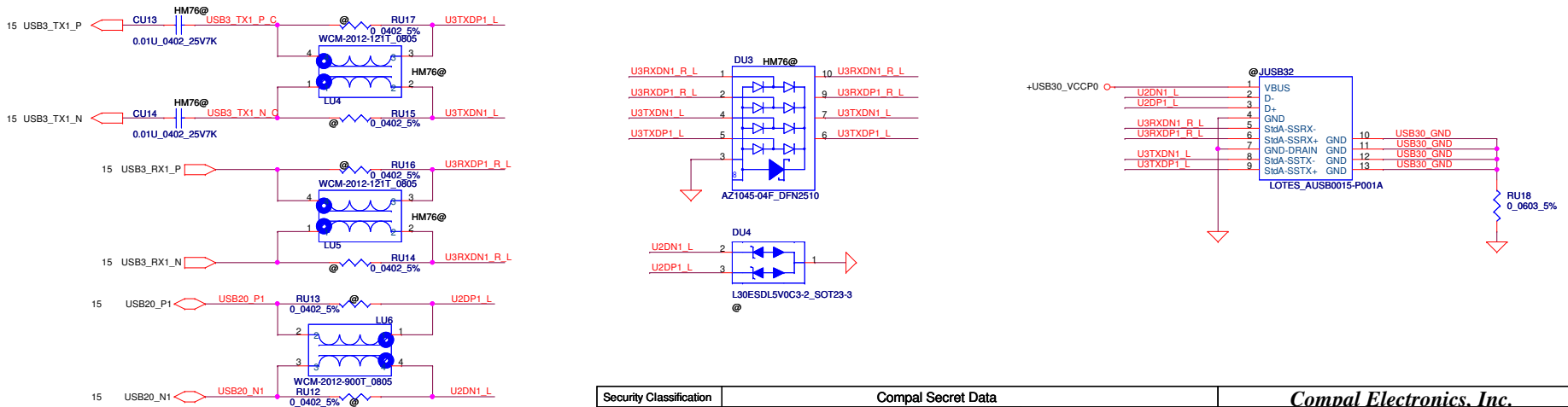
Port 0 : Left USB3.0



## USB3.0 Port 1

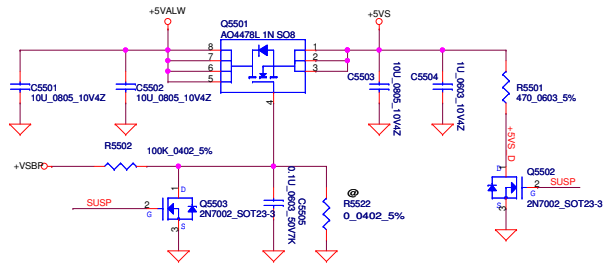
USB3.0 Port1

Port 1 : Left USB3.0

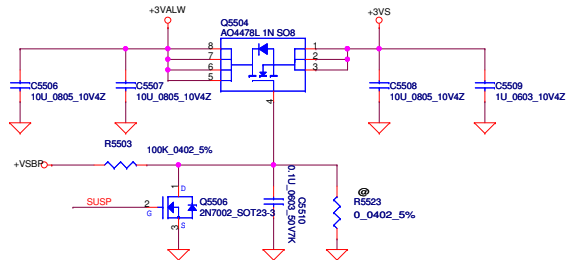


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				Power share ENE3810	
				Size	
				Document Number	
				QAL30 LA-8061P MB	
				Rev	
				0.1	
Date:				Friday, January 13, 2012	
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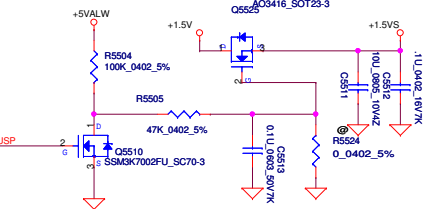
### +5VALW to +5VS



### +3VALW to +3VS

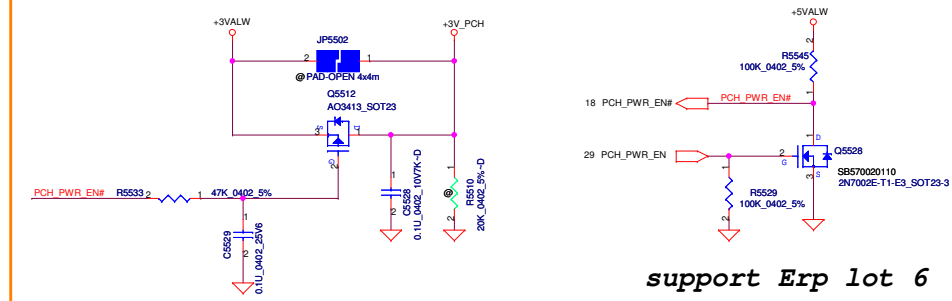


### +1.5V To +1.5VS

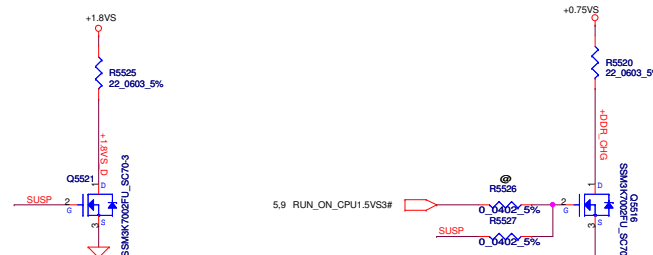
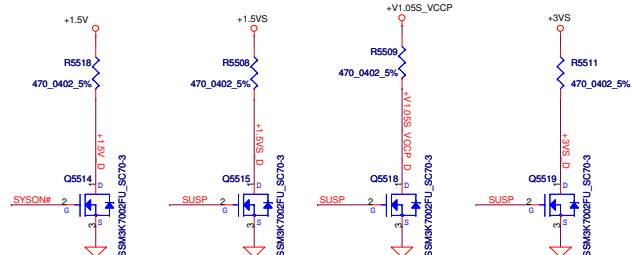


CHECK WITH CPU memory power

### +3VALW to +3V\_PCH

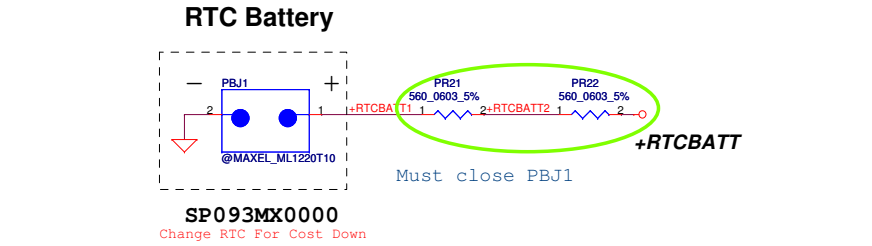
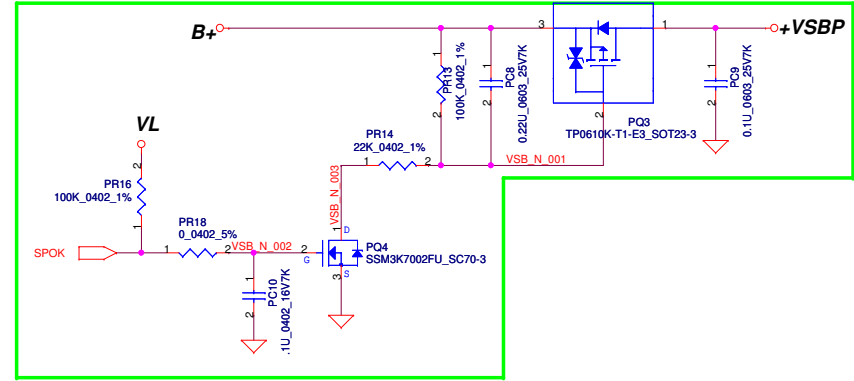
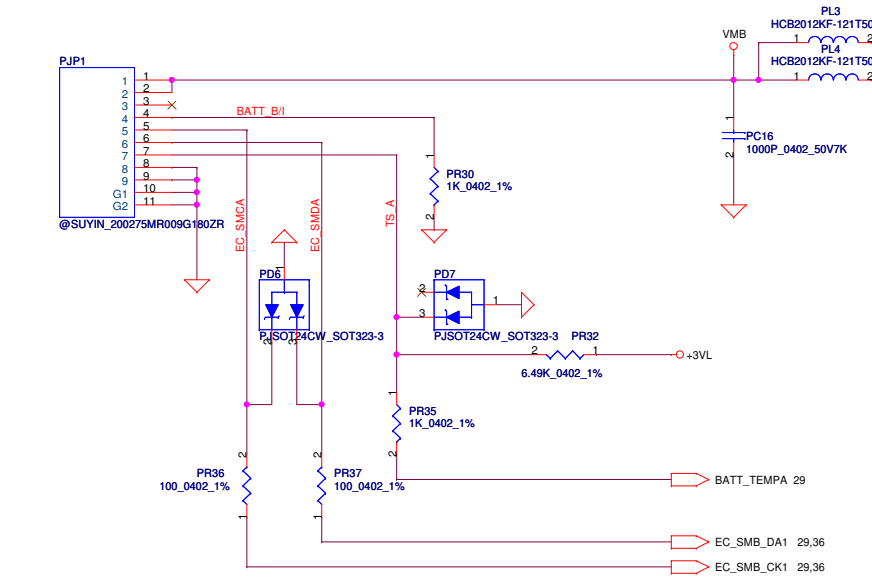
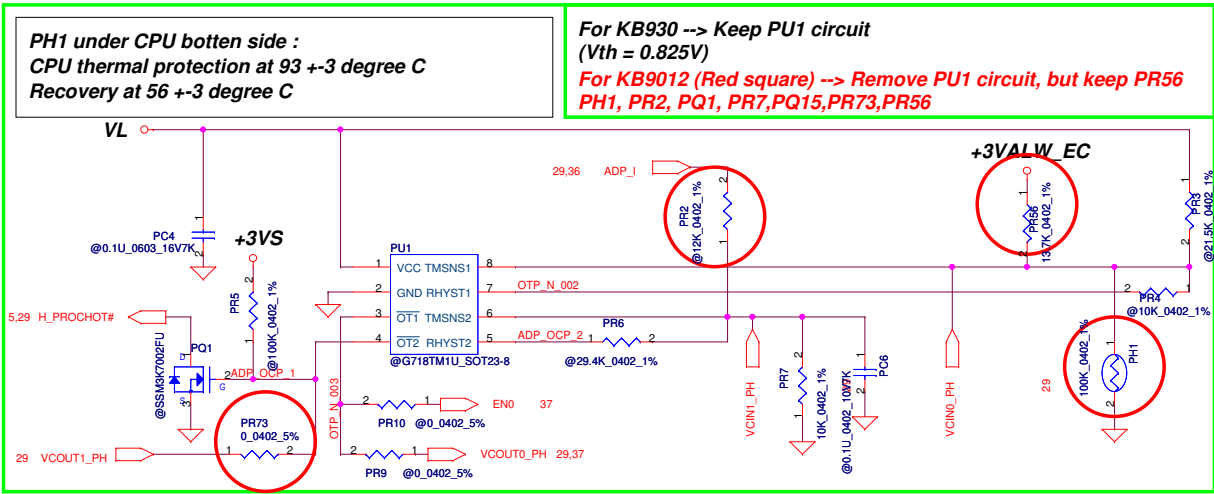
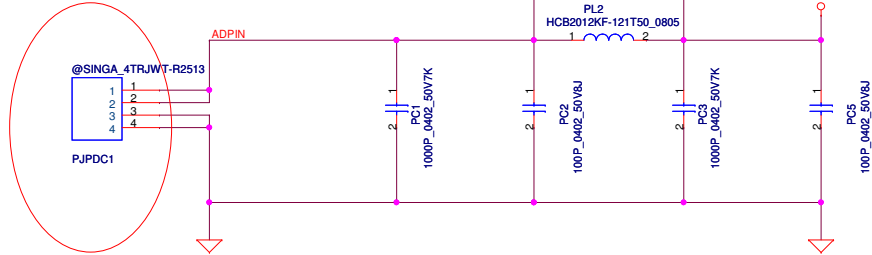


support Exp lot 6

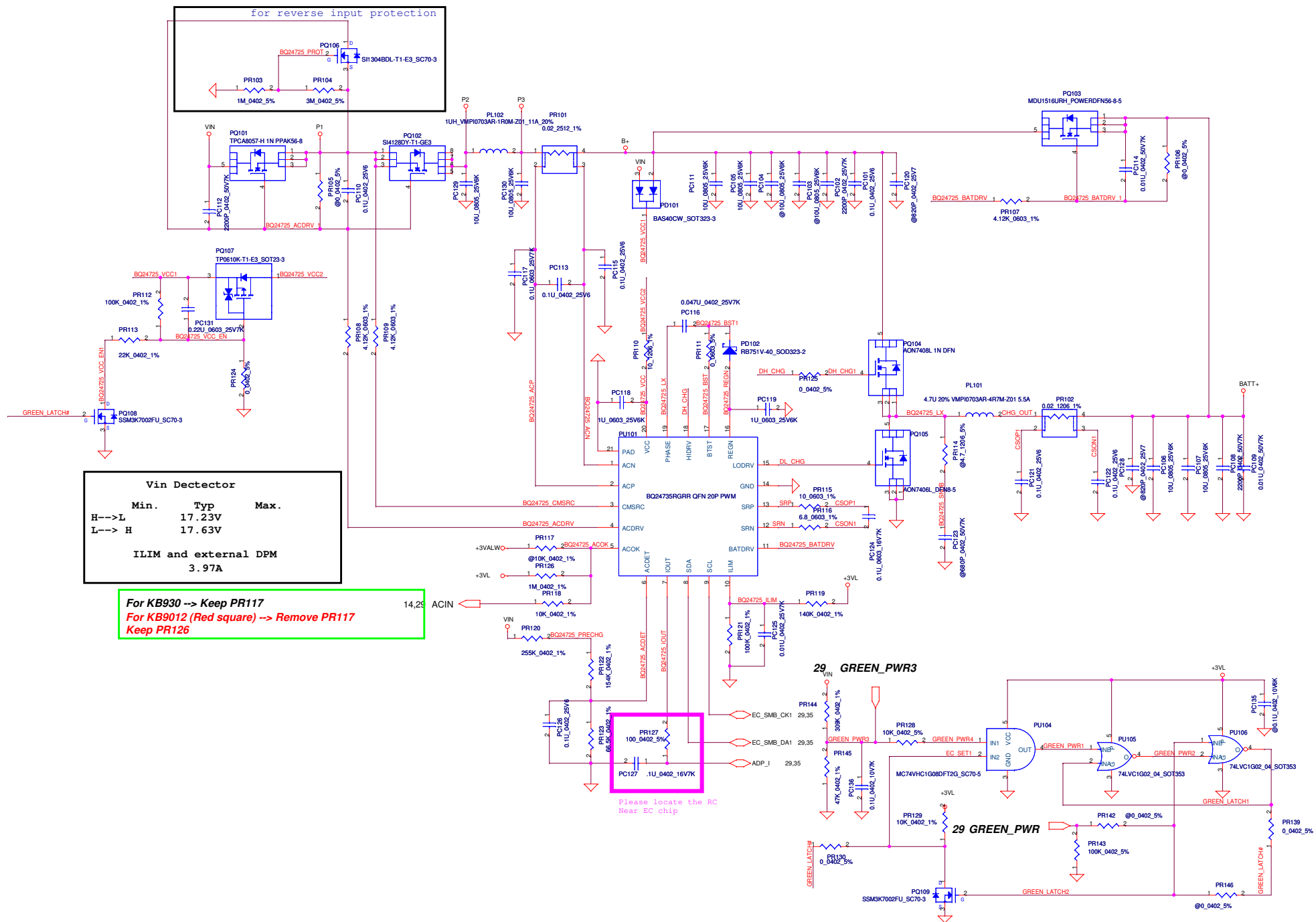


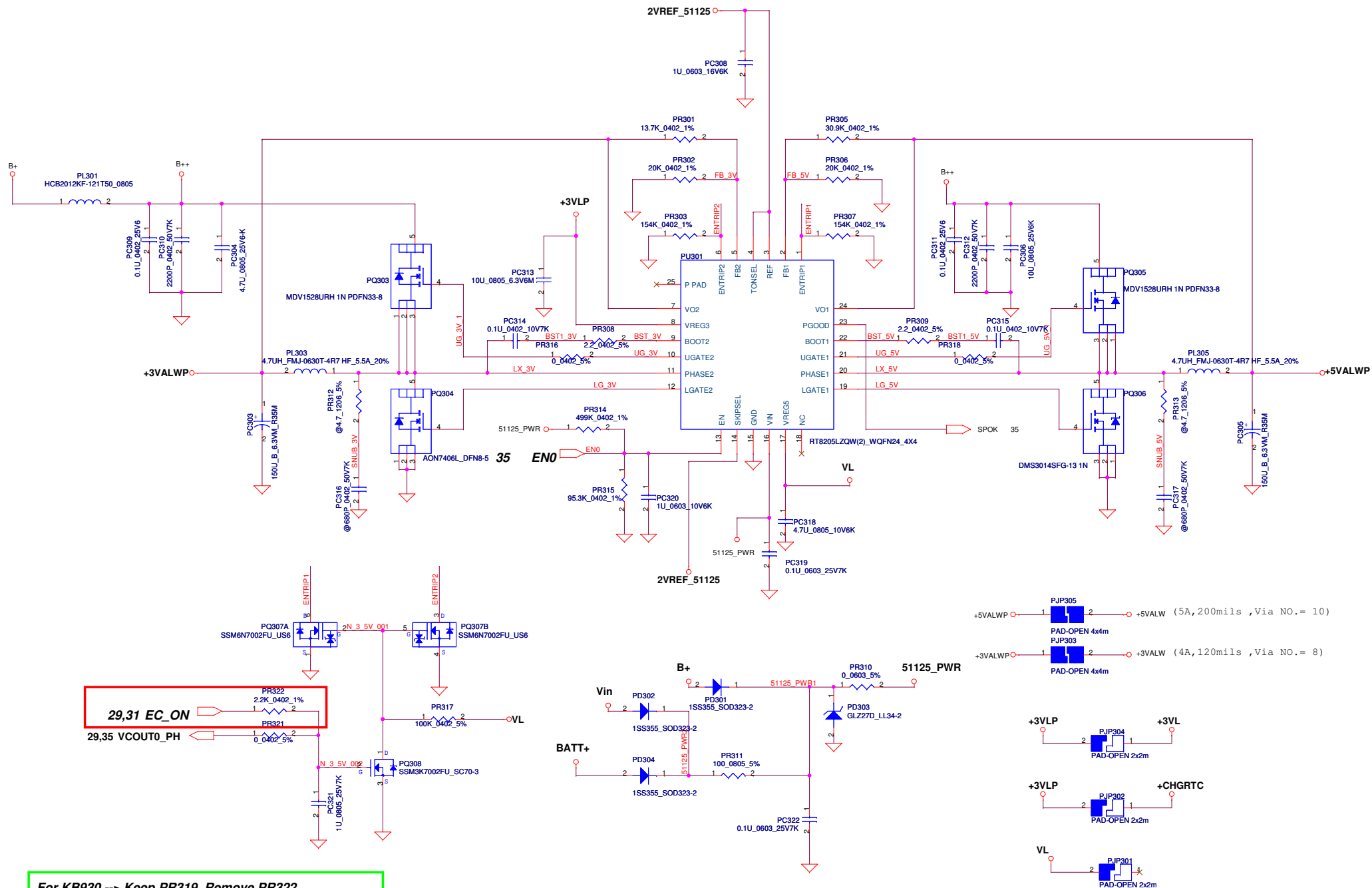
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				Date: Friday, January 13, 2012
				Sheet 34 of 46

DCIN jack P/N:DC301008L00,  
need doble confirm P/N with ME

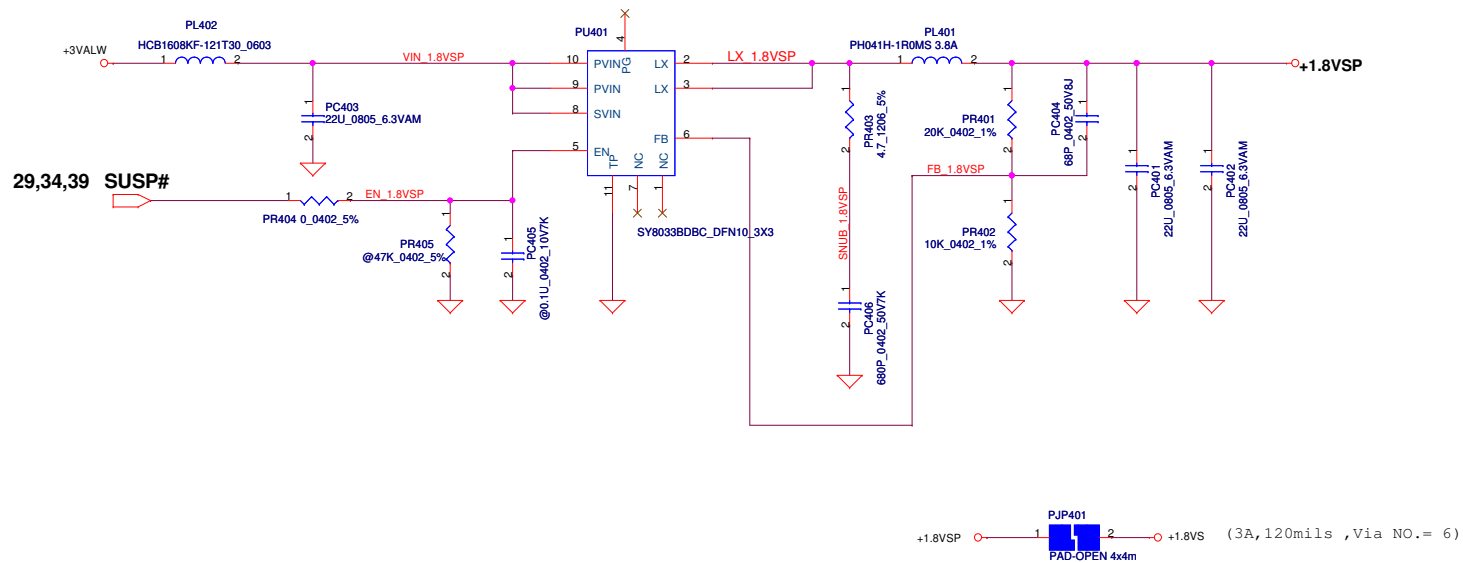


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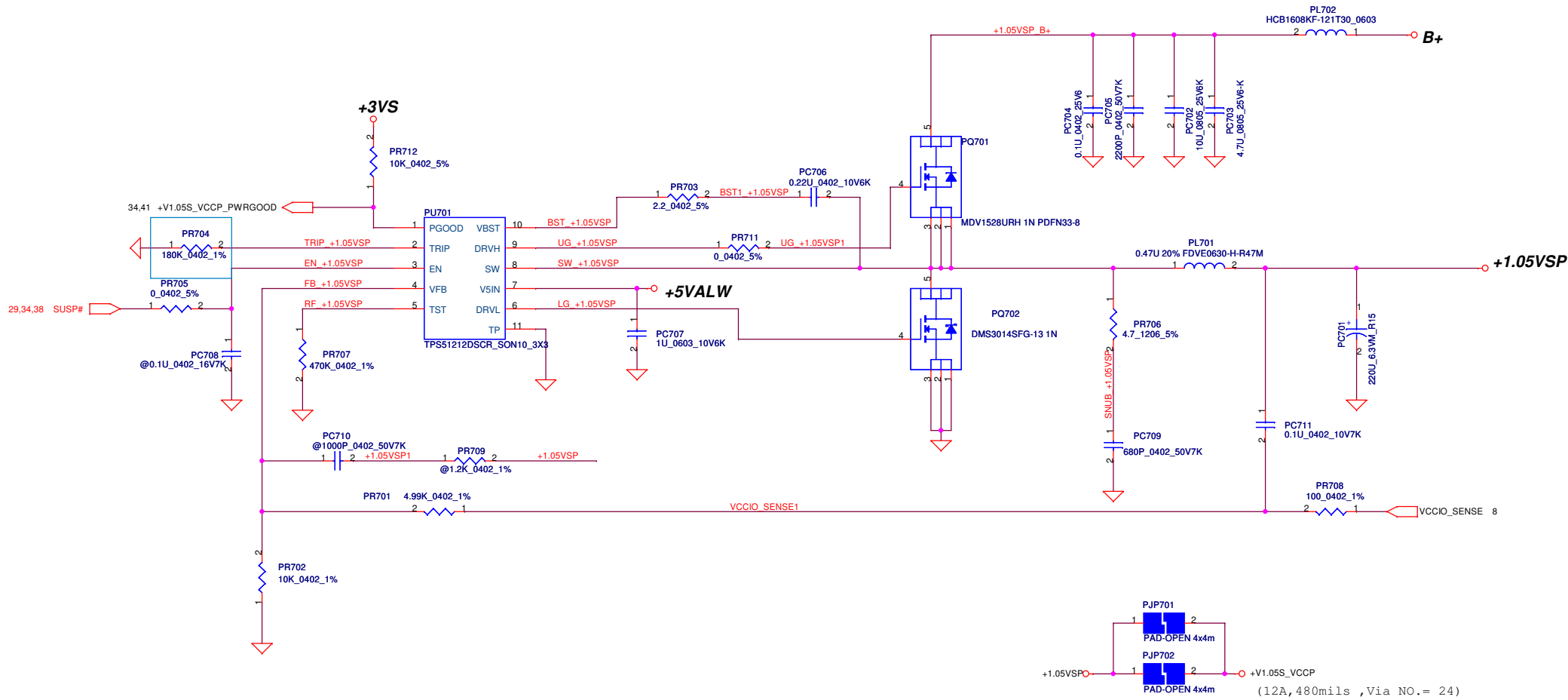




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				Rev	0.1



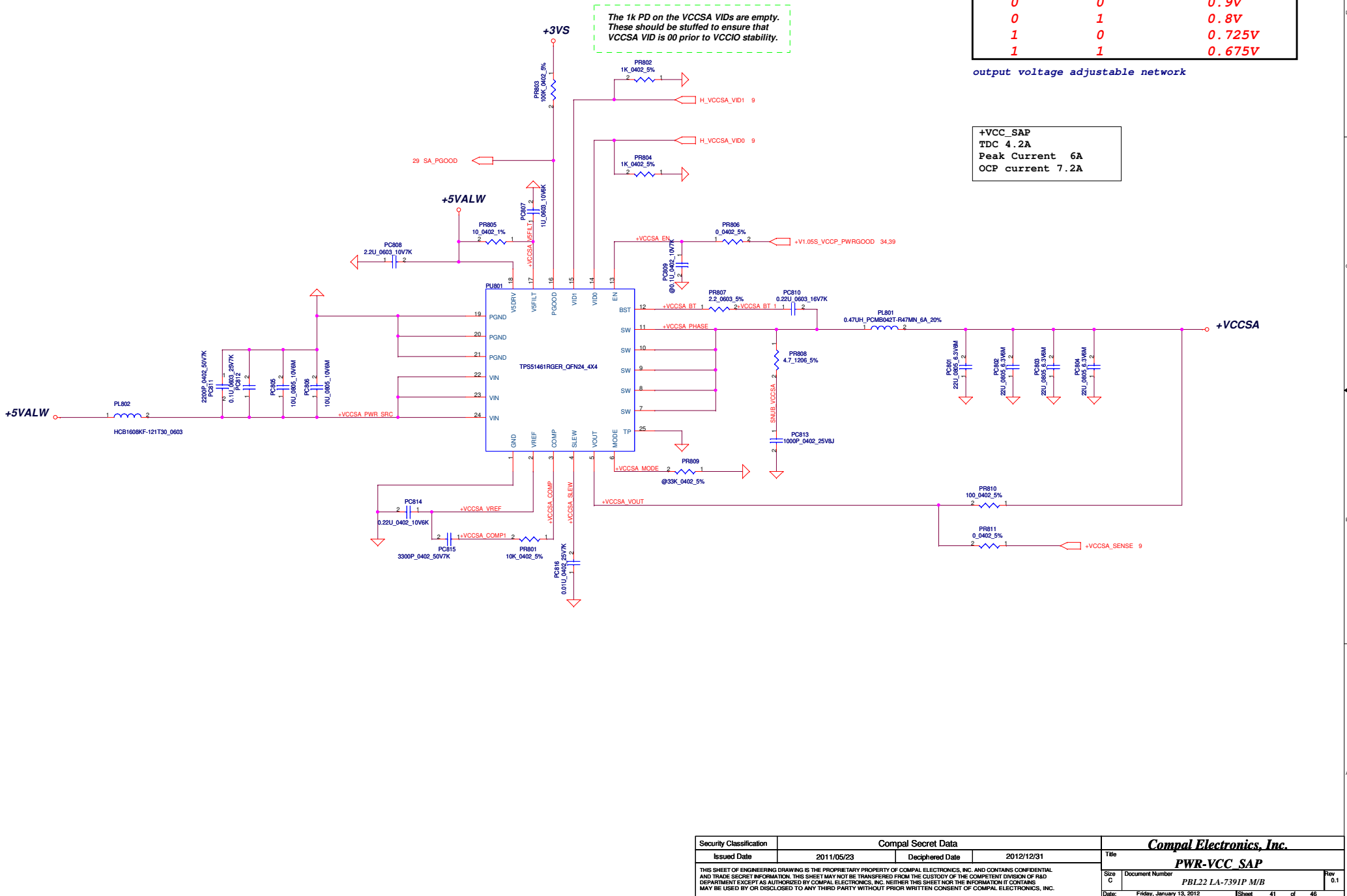
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

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				Date: Friday, January 13, 2012
				Sheet 41 of 46

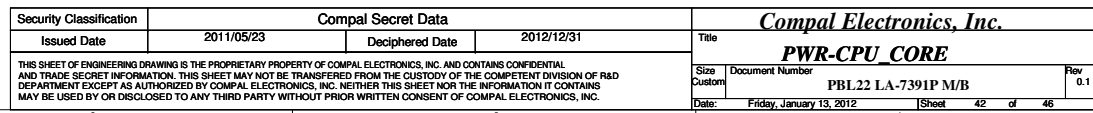
+5VS 

VSPA, VSNA to GND (HW side). FBA and COMPA are short.

VSPA, VSNA to GND (HW side). FBA and COMPA are short.

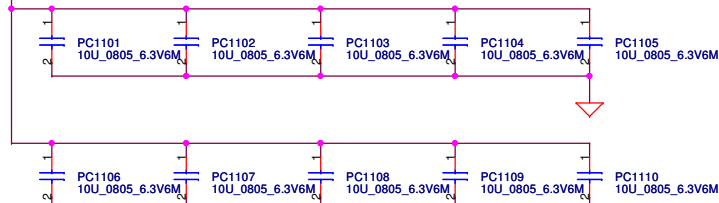
CSREFA, TSNSA, IOUTA to GND. CSCOMPA, CSSUMA, DROOPA are short.

DIS only:  
All AXG components are @.  
Except  
PR272 and PR273 are 0ohm.  
PC223, PC226, PR202 are 0ohm.  
PC220, PC215, PR206 are 0ohm.

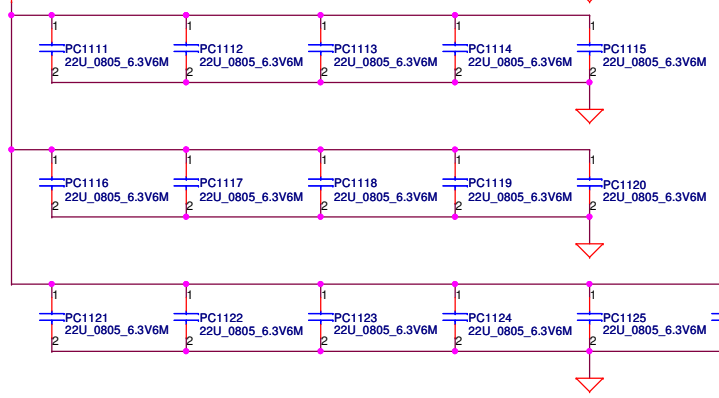




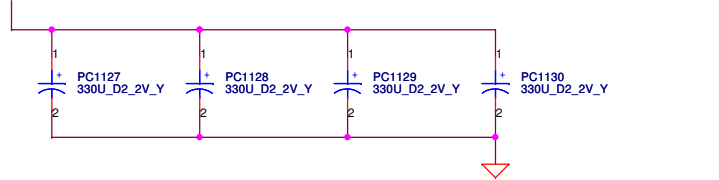
+VCC\_CORE



+VCC\_CORE



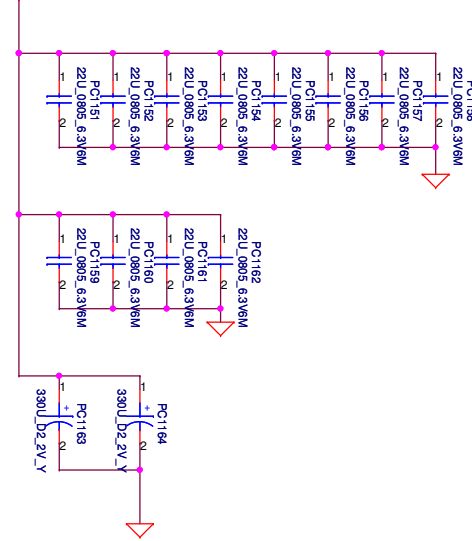
+VCC\_CORE



+VCC\_CORE

+GFX\_CORE

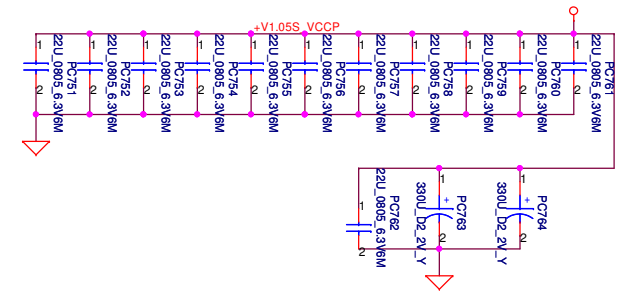
+GFX\_CORE



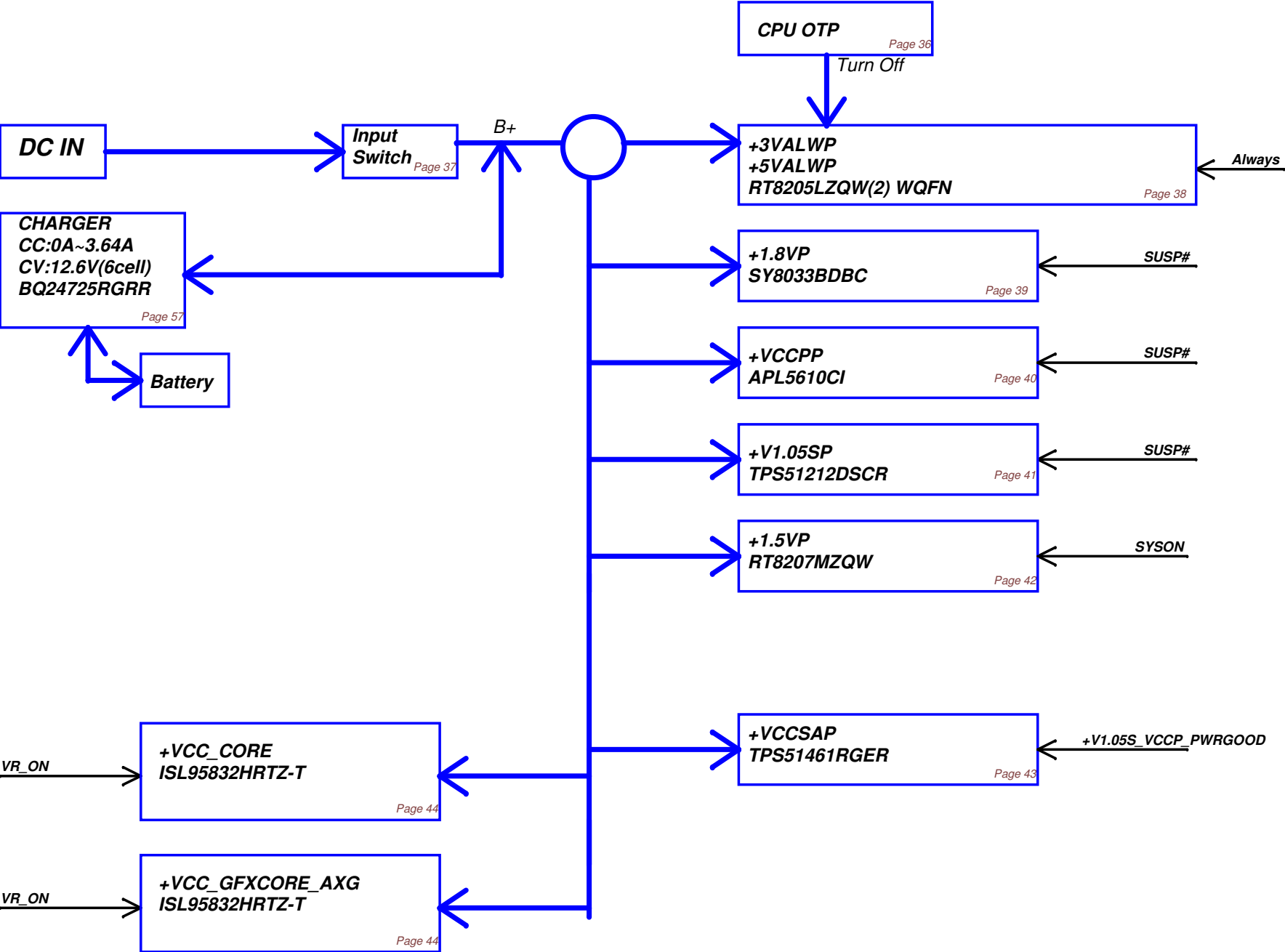
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

+V1.05S\_VCCP



Power block



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1					PR504 change from 15K to 15.4K		
2					charger IC change form bq24725A to bq24735		
3					PQ104,PQ303,PQ305,PQ701 charge form SIS412DN to MDW1528URH		
4					PQ306 charge from AON7702L to FDMC7692S		

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